



Q17H4-AD/ B15H4-AD

Rev:1.1 **ECS**
CONFIDENTIAL

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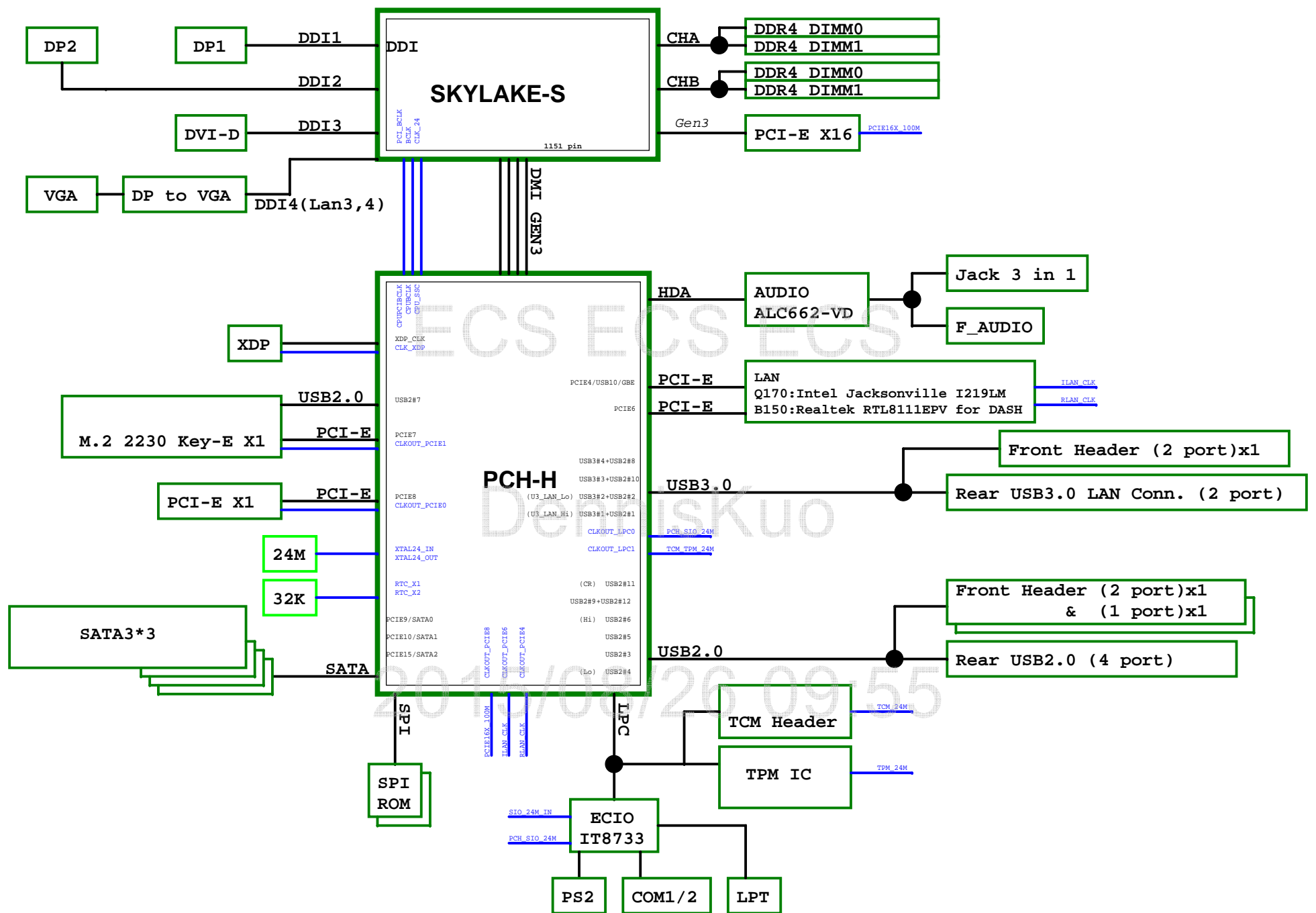
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sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCle/ LAN	PCle	PCle	PCle
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCle/ LAN	PCle	PCle	PCle
Q150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	N/A	LAN Only	PCle/ LAN	PCle	PCle	PCle
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCle	PCle/ LAN	PCle/ LAN	PCle	PCle	PCle
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCle	USB3/ PCle	USB3/ PCle	USB3/ PCle/ LAN	PCle/ LAN	PCle	PCle	PCle
Q170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3/ PCle	USB3/ PCle	USB3/ PCle	USB3/ PCle/ LAN	PCle/ LAN	PCle	PCle	PCle

sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports	
H110	PCle/ LAN	PCle	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A		0
B150	PCle/LAN	PCle/ SATA*	PCle	PCle/ LAN	SATA*/ LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A		0
Q150	PCle/LAN	PCle/ SATA	PCle	PCle/ LAN	SATA*/ LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A		0
H170	PCle/LAN	PCle/ SATA	PCle	PCle/ LAN	SATA*/ LAN	SATA*/ LAN	SATA	SATA	SATA	SATA	PCle	PCle		2
Z170	PCle/LAN	PCle/ SATA	PCle	PCle/ LAN	SATA*/ LAN	SATA*/ LAN	SATA	SATA	SATA	SATA	PCle	PCle		3
Q170	PCle/LAN	PCle/ SATA	PCle	PCle/ LAN	SATA*/ LAN	SATA*/ LAN	SATA	SATA	SATA	SATA	PCle	PCle		3

** SATA P0/P1 can be configured to PCIe Ports 9/10 or 13/14.

Intel® RST for PCIe Storage port configurable as SATA express x2 or M2 x2/x4.



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPP_D7	3VSB	GPP_D7_CASEOPEN	GPI
GPP_D6	3VSB	GPP_D6_BIOSWP	GPI
GPP_D5	3VSB	GPP_D5_BIOS_WP	GPI
GPD10	ATX_3VSB	GPD10	SLP_S5
GPD2	ATX_3VSB	ILAN_WAKE_L	LAN_WAKE#
GPD0	ATX_3VSB	RLAN_PWR_EN	BATLOW#
GPD11	ATX_3VSB	LAN_DIS_L	LANPHYPC
GPP_A12	3VSB	GPP_A12_TPM	GPI
GPP_A11	3VSB	LPC_PME_L	PME#
GPP_G13	VCC3	HDPANEL_DETECT	GPI
GPP_A14	VCC3	LPCPD_L	SUS_STAT#
GPP_A0	VCC3	KBRST_L_RC	RCIN#
GPP_A6	VCC3	SERIRQ	SERIRQ
GPP_A5	N/A	LPC_FRAME_L	LFRAME#
GPP_A1	N/A	LPC_LAD0	LAD0
GPP_A2	N/A	LPC_LAD1	LAD1
GPP_A3	N/A	LPC_LAD2	LAD2
GPP_A4	N/A	LPC_LAD3	LAD3
GPP_A9	N/A	PCH_SIO_24M	CLKOUT_LPC0
GPP_A10	N/A	TCM_TPM_24M	CLKOUT_LPC1
GPP_B3	VCC3	BT_DISABLE_L	GPI
GPP_B17	VCC3	WLAN_DISABLE_L	GPI
GPP_E8	VCC3	SATALED_L	GPI
GPP_E9	+USBVCC3	USB_OC0_L	GPI
GPP_E10	+USBVCC2	USB_OC1_L	GPI
GPP_F15	+USB3VCC	USB_OC4_L	GPI
GPP_F16	3VSB	GPP_F16	GPI
GPP_F17	+USBVCC1	USB_OC6_L	GPI
GPP_F18	+USBVCC5	USB_OC7_L	GPI
GPP_I0	N/A	DDPB_HPD0	GPI
GPP_I1	N/A	DDPC_HPD1	GPI
GPP_I2	N/A	DDPD_HPD2	GPI
GPP_G23	3VSB	GPP_G23	GPI
GPP_F22	VCC3	GPP_F22_PCIEIRST	GPI
GPP_C3	3VSB	SML0_CLK	SML0CLK
GPP_C4	3VSB	SML0_DATA	SML0DATA
GPP_C6	3VSB	SML1_CLK	GPI
GPP_C7	3VSB	SML1_DATA	GPI
GPP_C0	3VSB	SMBCLK_STBY	SMLCLK
GPP_C1	3VSB	SMBDATA_STBY	SMLDATA
GPP_C16	3VSB	I2C0_SDA	GPI
GPP_C17	3VSB	I2C0_SCL	GPI
GPP_C18	3VSB	I2C0_ALERT_L	GPI
GPD9	ATX_3VSB	PCH_RI_L	SLP_WLAN#
GPP_I5	VCC3	DDIB_CTRLCLK	GPI
GPP_I6	VCC3	DDIB_CTRLDATA	GPO
GPP_I7	VCC3	DDIC_CTRLCLK_DP	GPI
GPP_I8	VCC3	DDIC_CTRLDATA_DP	GPO
GPP_I9	VCC3	DDID_CTRLCLK	GPI
GPP_I10	VCC3	DDID_CTRLDATA	GPO
GPP_H0	3VSB	ILAN_CLKREQ	GPI
GPP_B13	N/A	PCH_PLTRST_L	PLTRST#
GPP_B14	N/A	PCH_SPKR	GPO
GPP_B6	3VSB	M2CLK_REQ1_L	GPI
GPP_E0	3VSB	GPP_E0_OBR	GPI

GPP_H14	3VSB	GPP_H14 (Acer reserve)	GPI
GPP_H15	3VSB	GPP_H15 (Acer reserve)	GPI
GPP_E11	+USBVCC0	USB_OC5_L	GPI

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP37	+DIMM_5VDUAL	SIO_LED1	FAN_TAC3(DI)
GP36	3VSB	GPP_E7_THERM	FAN_CTL3(DOD8)
GP35	+DIMM_5VDUAL	SIO_LED0	FAN_TAC4(DI)
GP34	3VSB	SUSWARN_L	SUSWARN#(DOD8)
GP33	3VSB	SUSACK_L	SUSACK#(DOD8)
GP32	ATX3VSB	DPWROK	DPWROK(DOD8)
GP31	3VSB	sleep mode wake up	
GP30	VCC	ATX_PWRGD	ATXPG(DI)
GP14	3VSB	SML1_CLK	VCORE_EN(DOD8)
N/A	3VSB	SML1_DATA	PCH_D1
GP13	VCC3	PCH_SYSPWROK	PWROK1(DOD8)
GP12	N/A	PCIRST1_L	PCIRST1#(DO8)
GP11	N/A	PCIRST2_L	PCIRST2#(DO8)
GP44	3VSB	SIO_PWRON_L	PWRON#(DOD8)
GP54	3VSB	LPC_PME_L	PME#(DOD8)
GP43	ATX5VSB	FP_PWRBTN_L	PANSWH#(DI)
GP42	ATX3VSB	ATX_PSON_L	PSON#(DOD8)
GP53	N/A	SLP_S4_L	SUSC#(DI)
GP40	3VSB	3VSBSW_L	3VSBSW#(DO8)
GP10	N/A	PCIRST3_L	PCIRST3#(DO8)
GP55	3VSB	RSMRST_L	RSMRST3#(DOD8)
GP16	3VSB	basic health function	

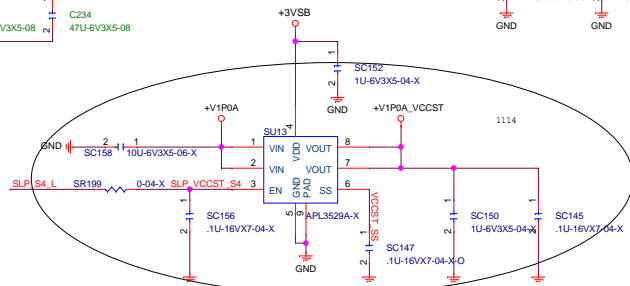
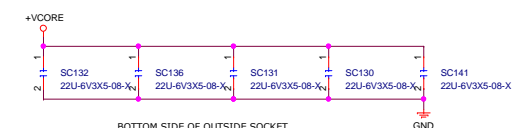
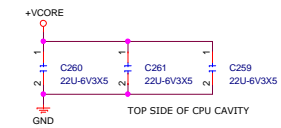
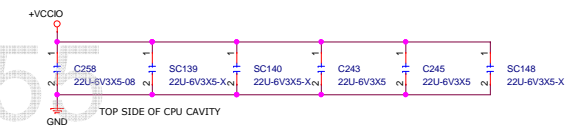
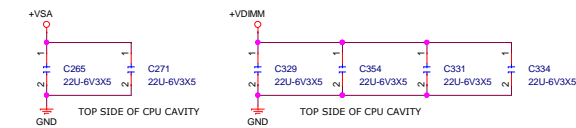
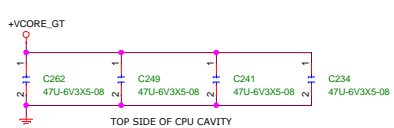
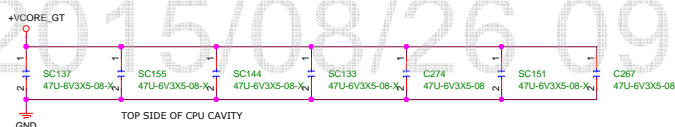
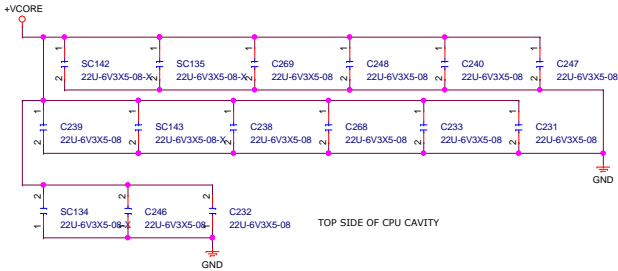
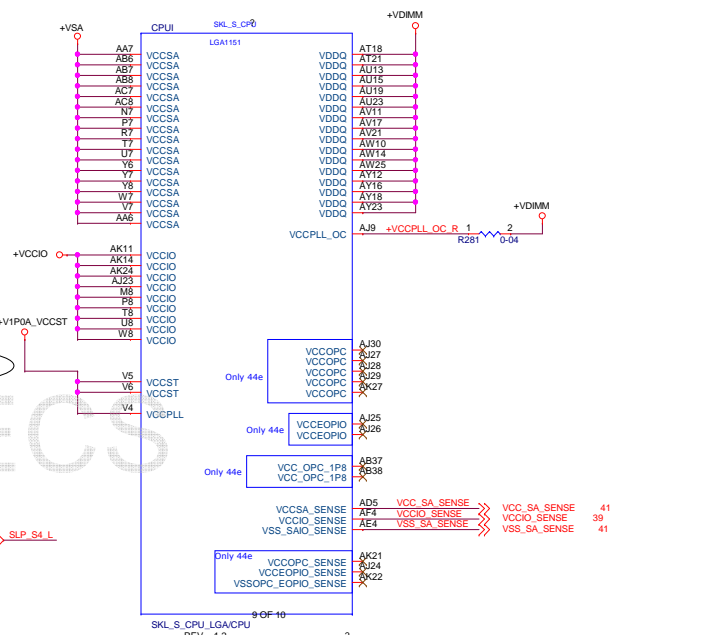
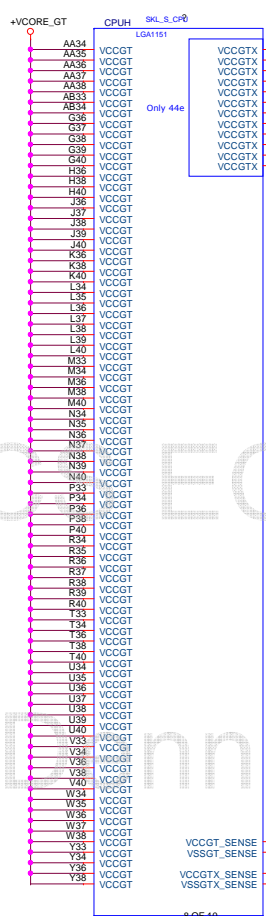
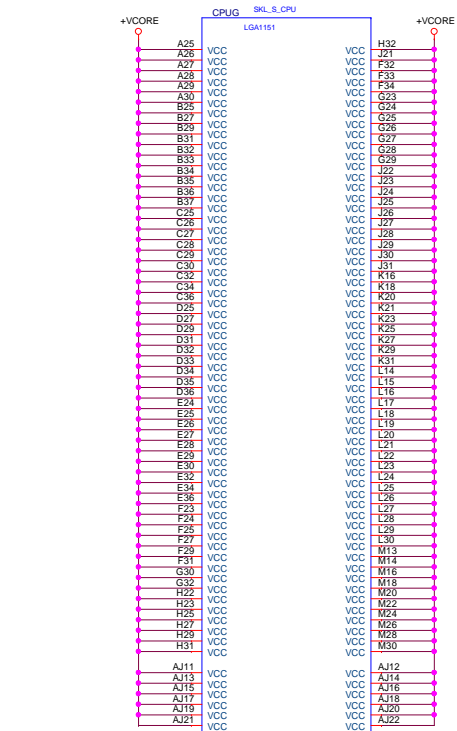
CPU-Strap

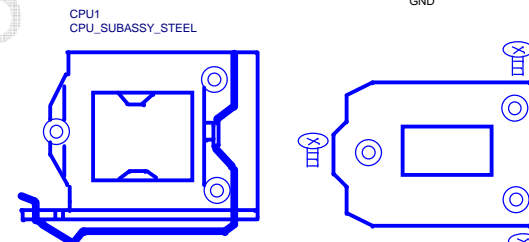
Pin Name	Usage	Default Status
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted	1 = (Default) Normal Operation
CFG1	CFG[1]: Reserved configuration lane	
CFG2:5:6	CFG[2]:1 = Normal operation CFG[6:5]:11 = 1 x16 PCI Express	PCIEL6X
CFG3	CFG[3]: Reserved configuration lane.	
CFG4	CFG[4]: eDP enable:	0 = Enable
CFG7	CFG[7]: PEG Training:	1 = (default) PEG Train immediately following RESET# de assertion.
CFG19:8	CFG[19:8]:Reserved configuration lanes.	
SPKR/GPP_B14	Top Swap Override	0 =Disable "Top Swap" mode. (Default)
GSPIO_MOSI/GPP_B18	No Reboot	0 =Disable the Reboot/transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS
SMBALERT#/GPP_C2	TLS Confidentiality	
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit BBS	0=SPI
SML0ALERT#/GPP_C5	eSPI or LPC	This pin is a pull-up resistor. This pin should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
HDA_SDO	Flash Descriptor Security Override	0 =Enable security measures defined in the Flash Descriptor. 1 =Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
DDPB_CTRLDATA/GPP_I6	Display Port B Detected	1 = Port B is detected.
DDPC_CTRLDATA/GPP_I8	Display Port C Detected	1 = Port C is detected.
DDPB_CTRLDATA/GPP_I10	Display Port D Detected	1 = Port D is detected.

- ◀ M_DATA A[0..63]
- ◀ M_CLK A P[0..3]
- ◀ M_CLK A N[0..3]
- ◀ M_CKE A[0..3]
- ◀ M_CS A L[0..3]
- ◀ M_ODT A[0..3]
- ◀ M_MA A[0..15]
- ◀ M_DQS A P[0..7]
- ◀ M_DQS A N[0..7]

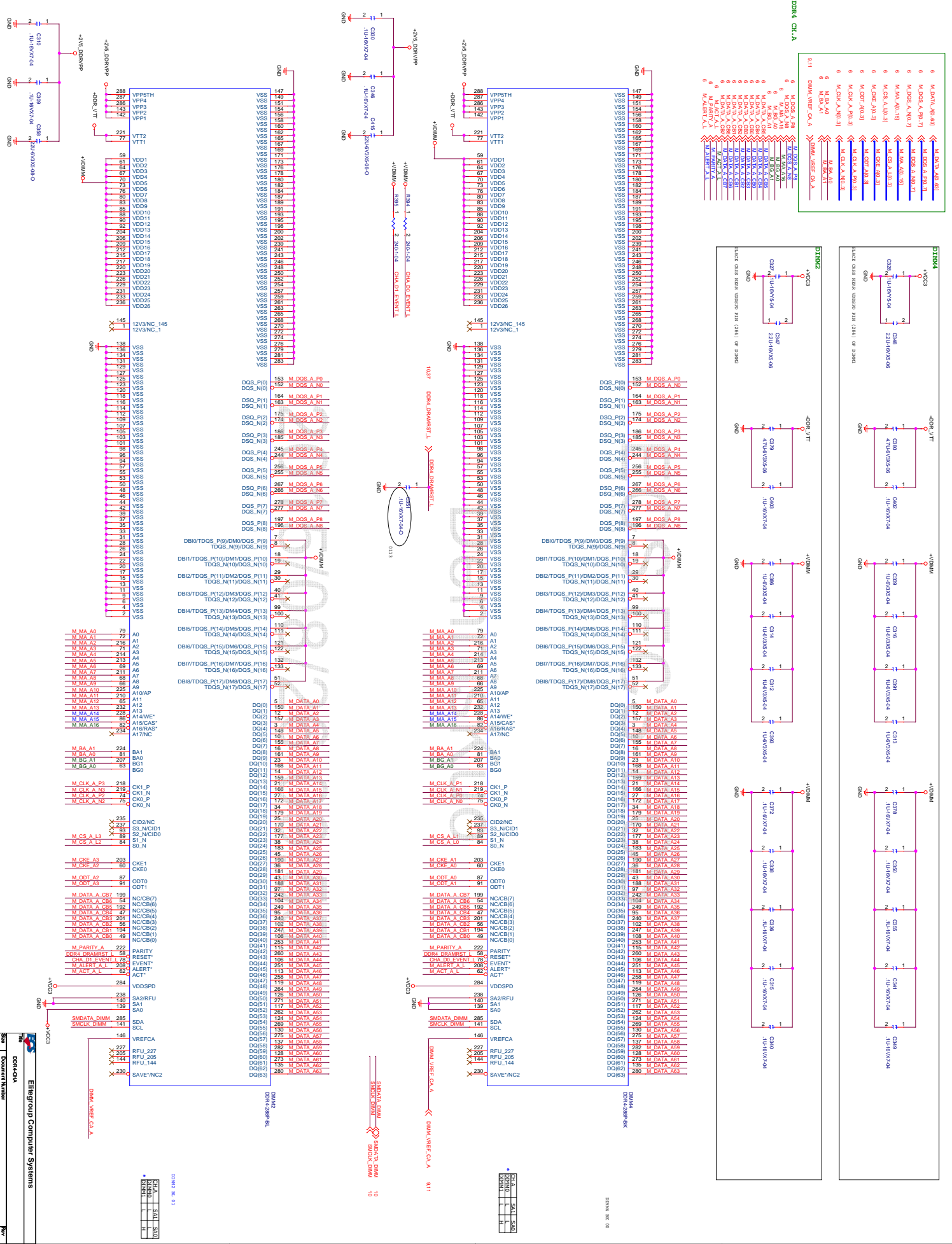
- « M_DATA_B[0..63]
- « M_CLK_B_P[0..3]
- « M_CLK_B_N[0..3]
- « M_CKE_B[0..3]
- « M_CS_B_L[0..3]
- « M_ODT_B[0..3]
- « M_MA_B[0..15]
- « M_DQS_B_P[0..7]
- « M_DQS_B_N[0..7]



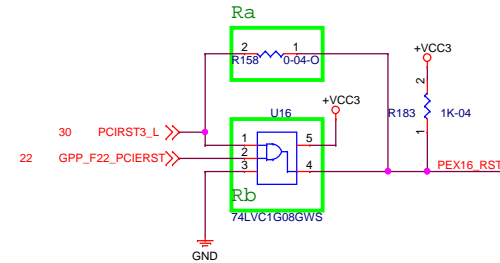
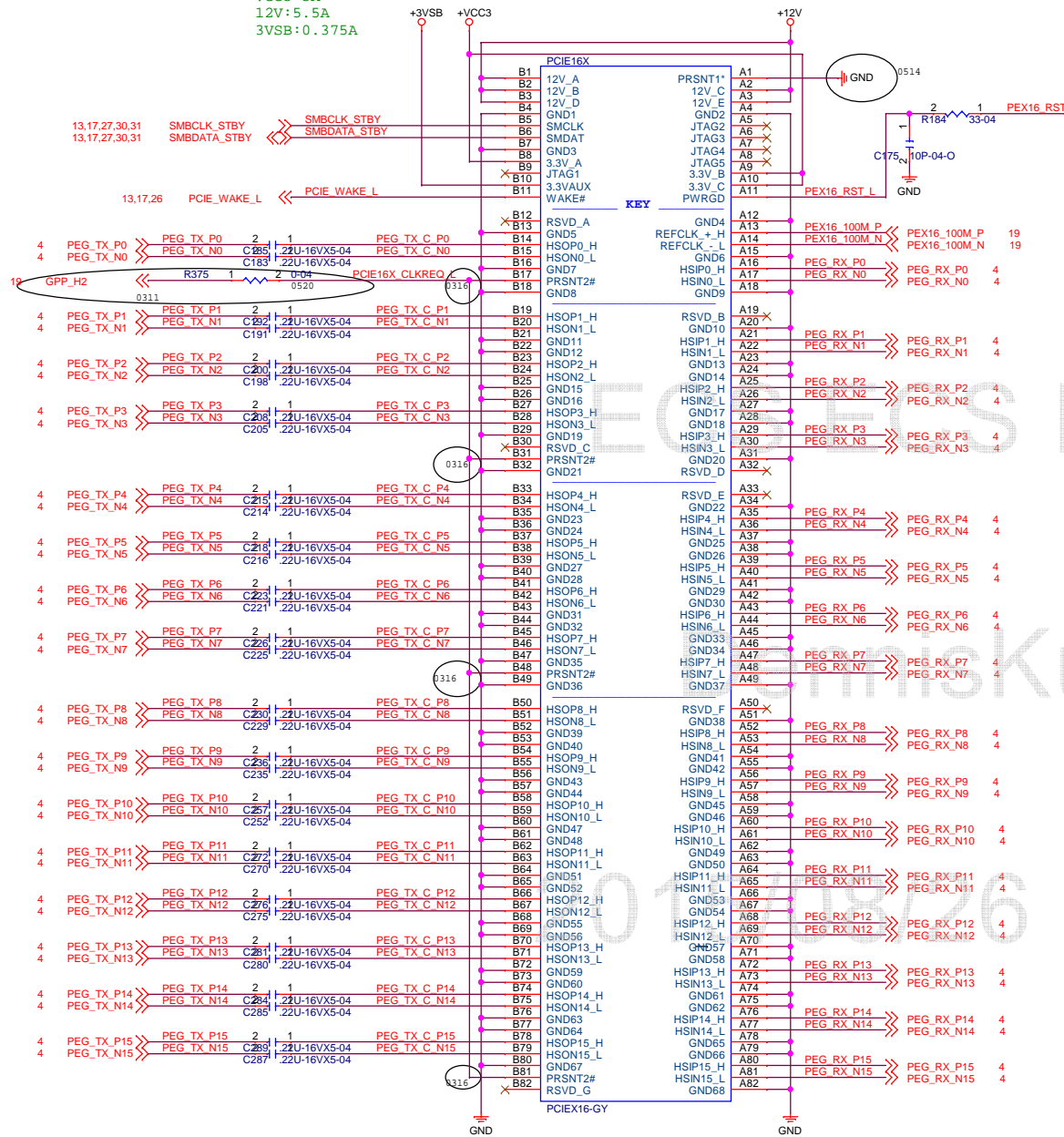




CPU Socket (SMD phase)
PN:11-018-115133
SOCKET.CPU..LGA 1151P SMD..G/F...BLACK.AZIF0049-P002C...HF.LEAD-FREE.LOTES

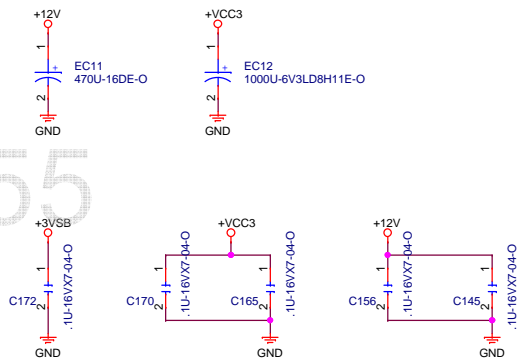


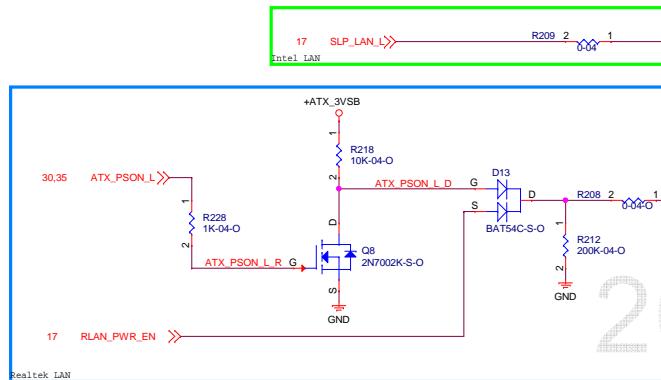
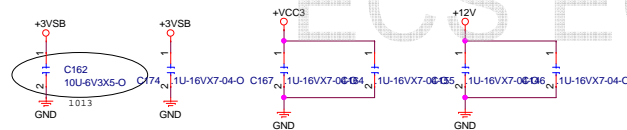
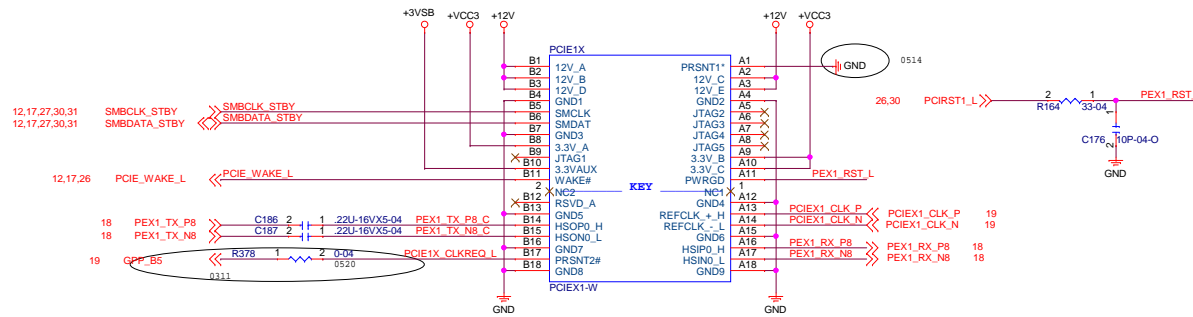
PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



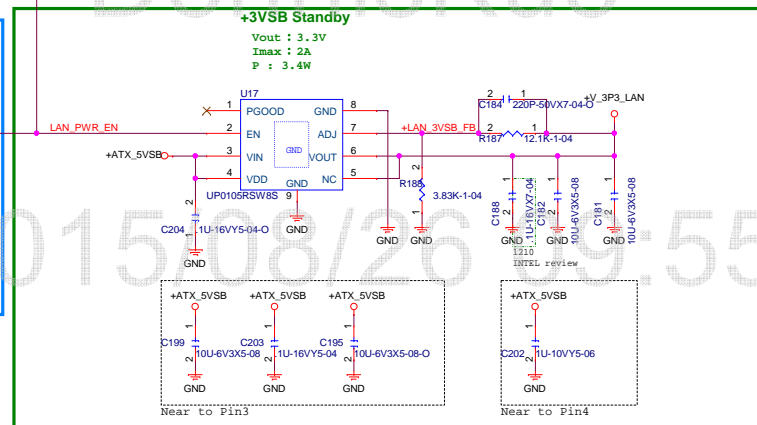
	Ra	Rb
GPIO PEG Reset	X	V
NO GPIO PEG Reset	V	X

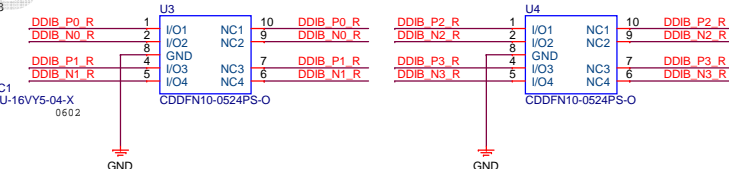
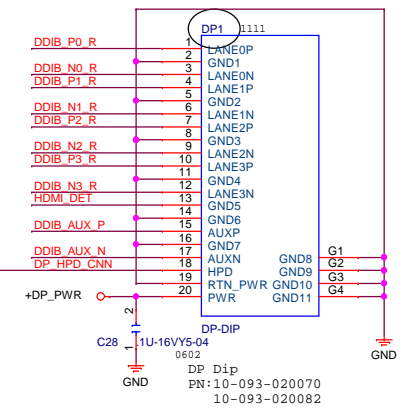
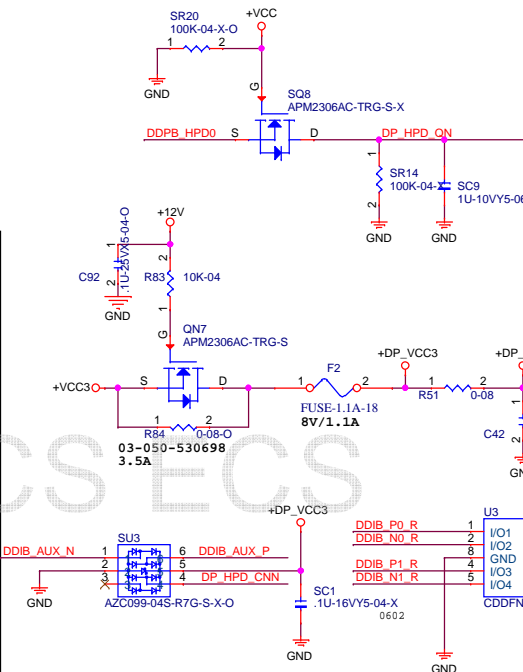
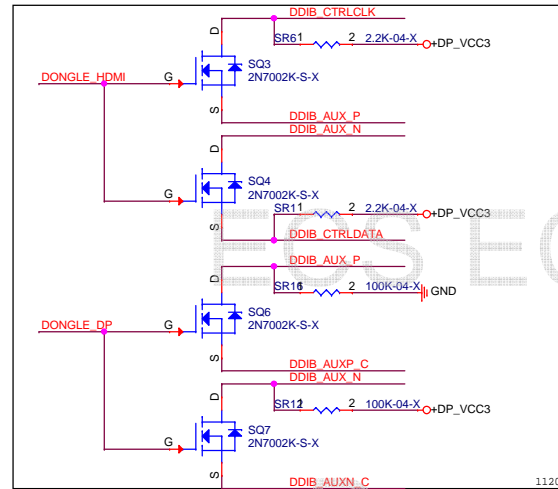
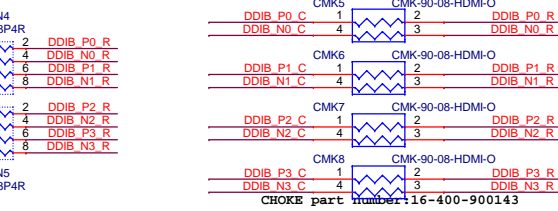
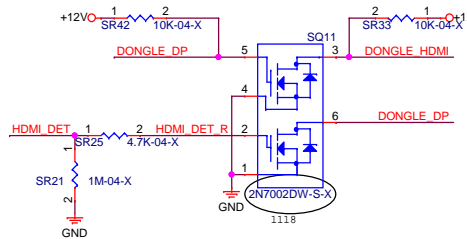
Between PCIE16 & PCIE1



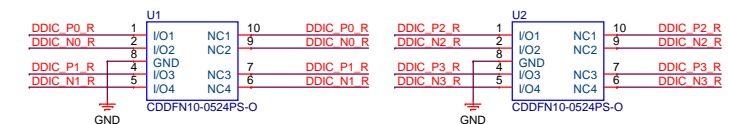
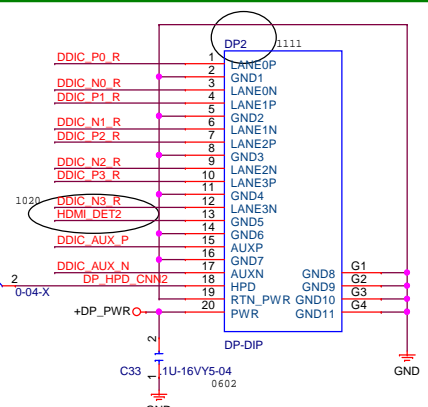
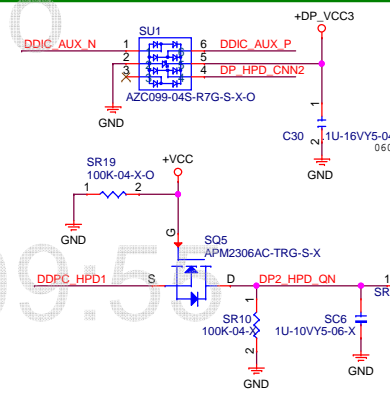
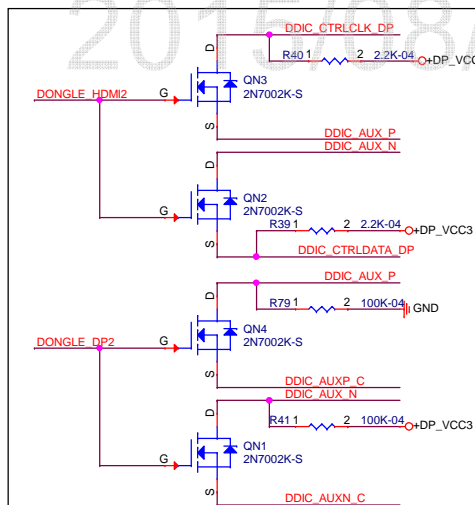
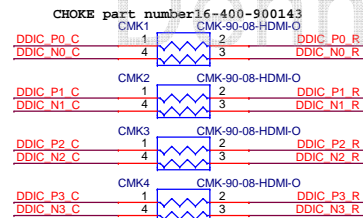
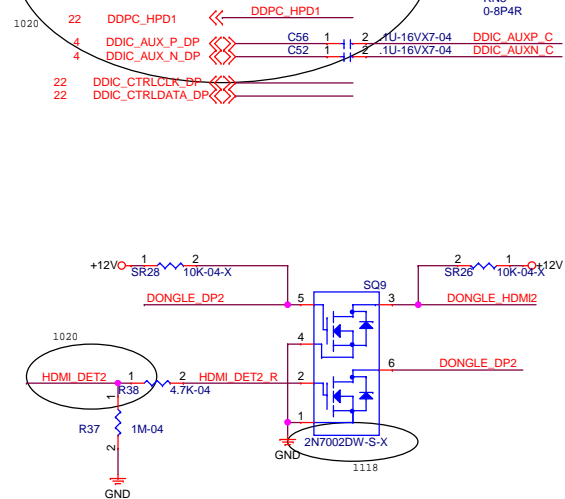
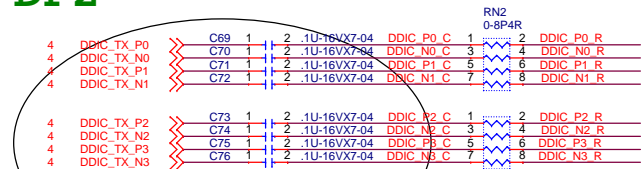


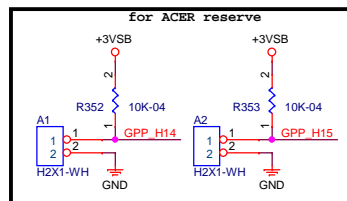
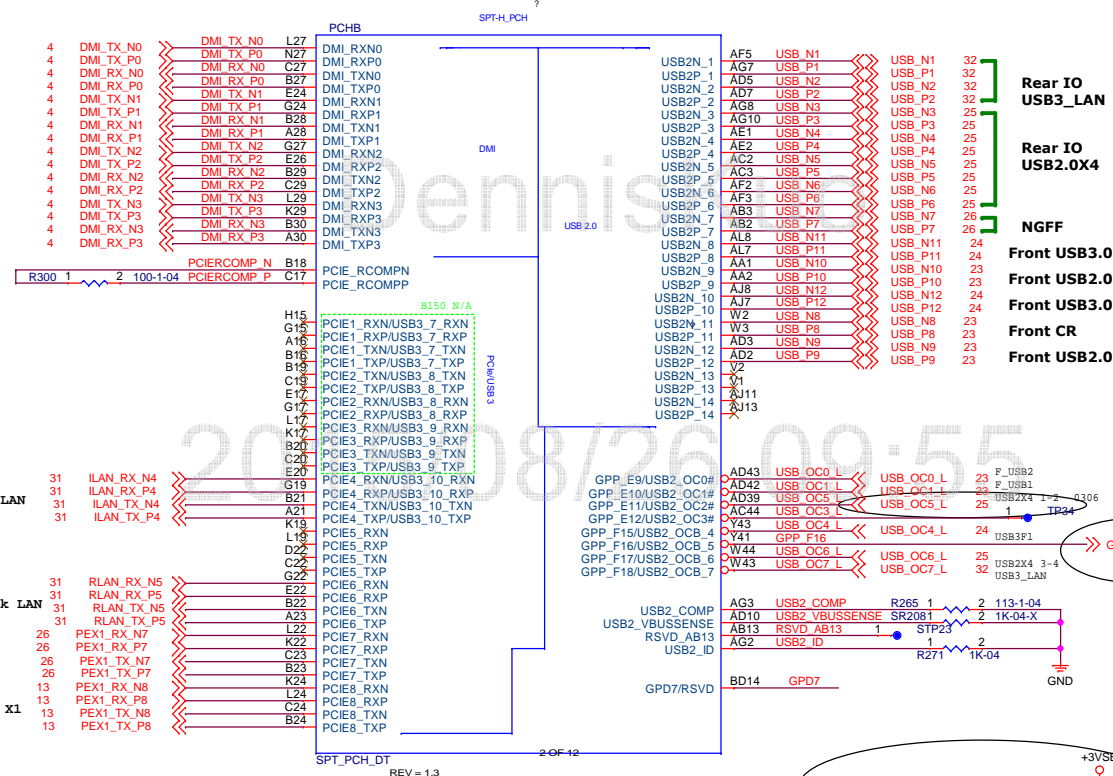
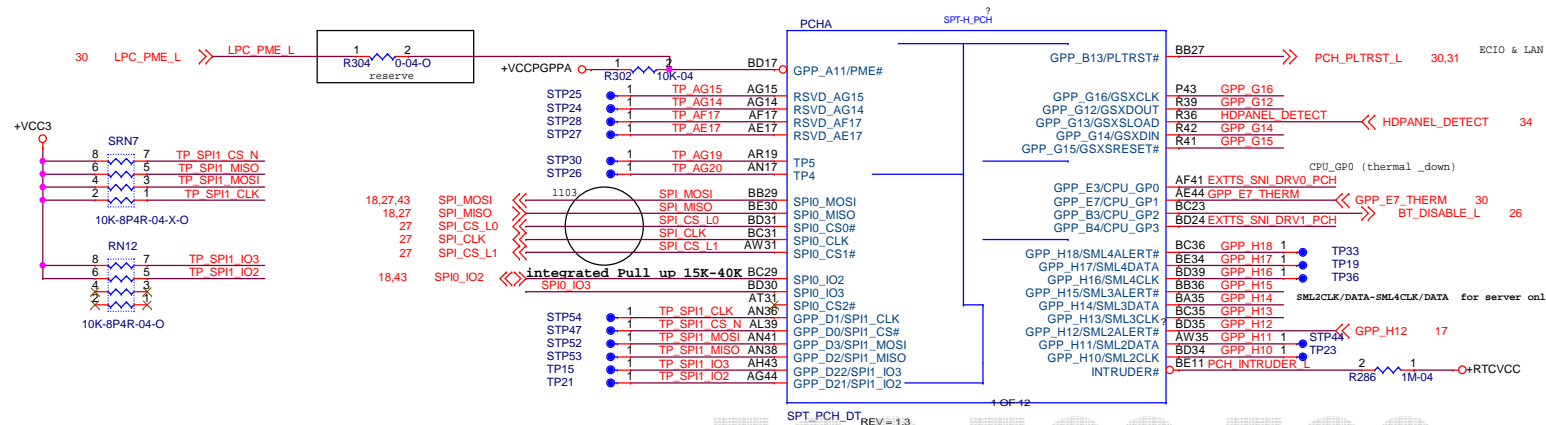
SLP_LAN_L	Intel LAN
RLAN_PWR_EN	Realtek LAN



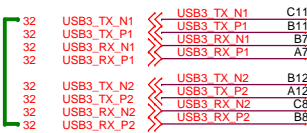


DP1
DP2

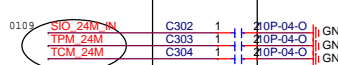
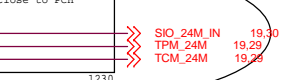
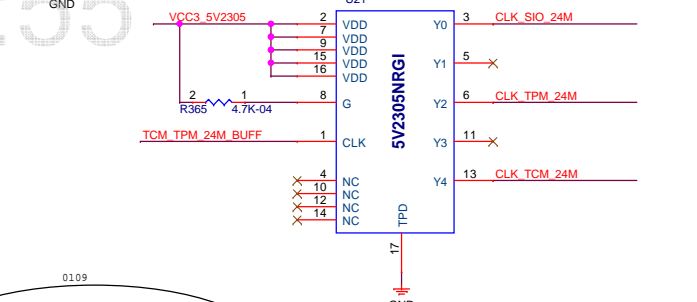
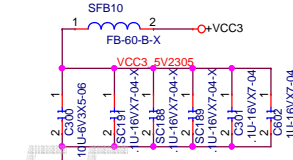
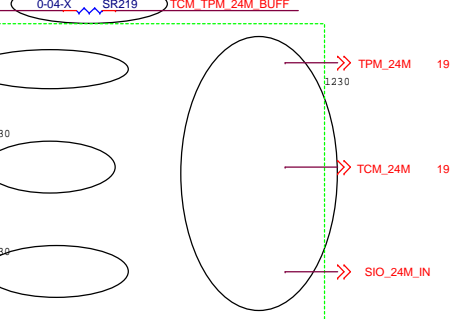
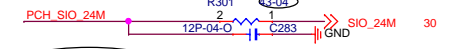
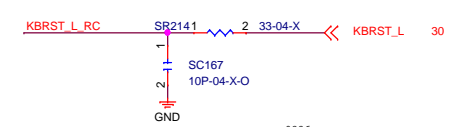
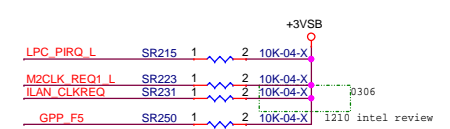
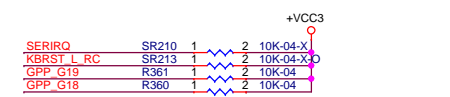
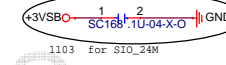
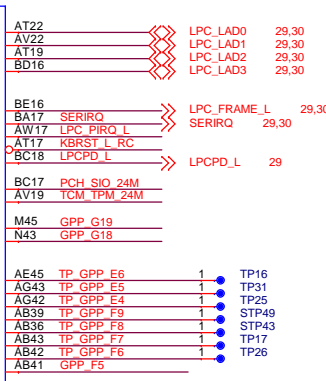
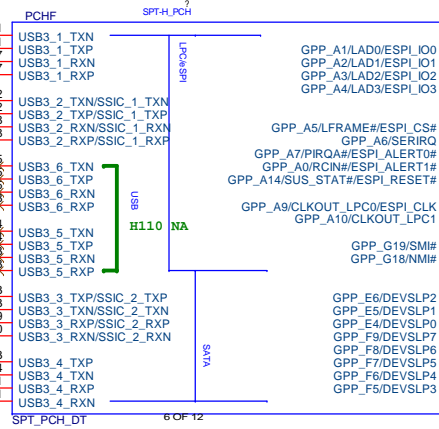
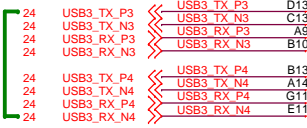


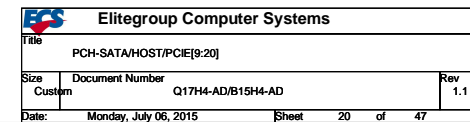


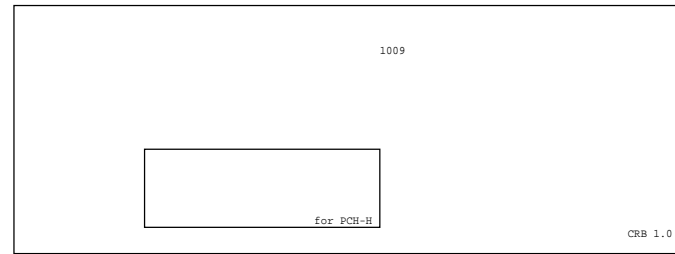
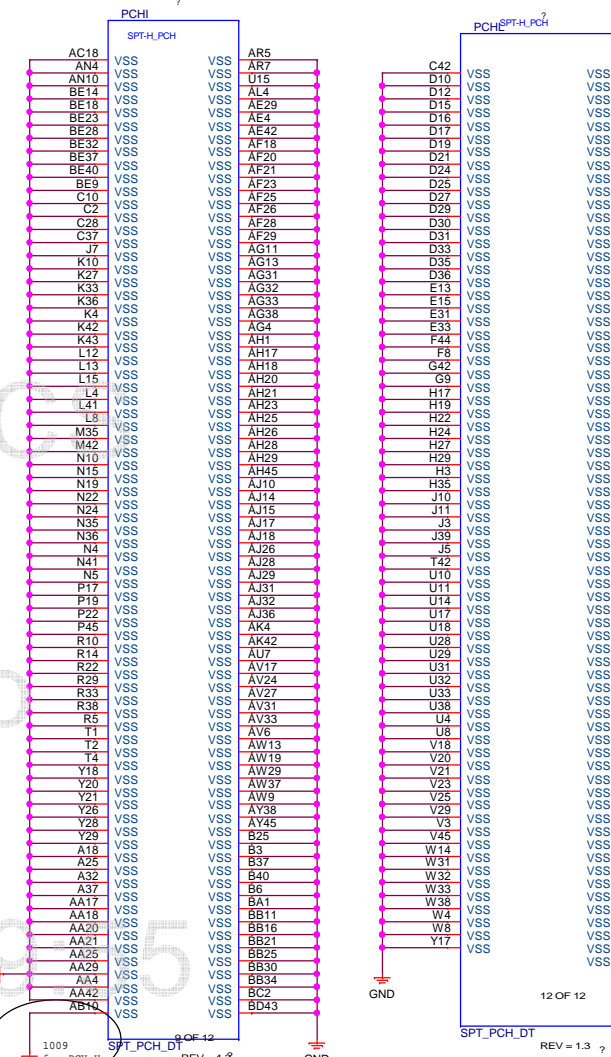
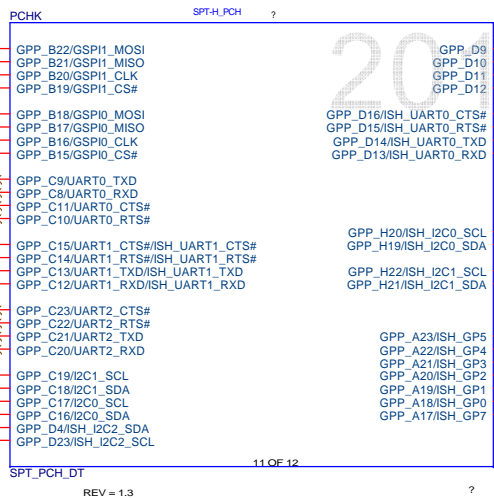
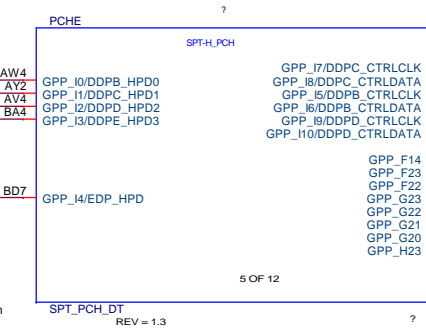
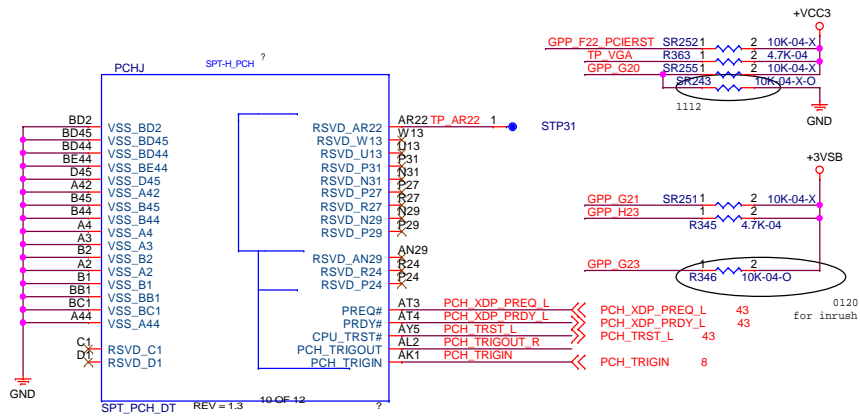
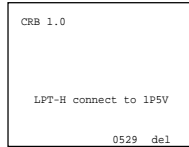
Rear IO USB3.0

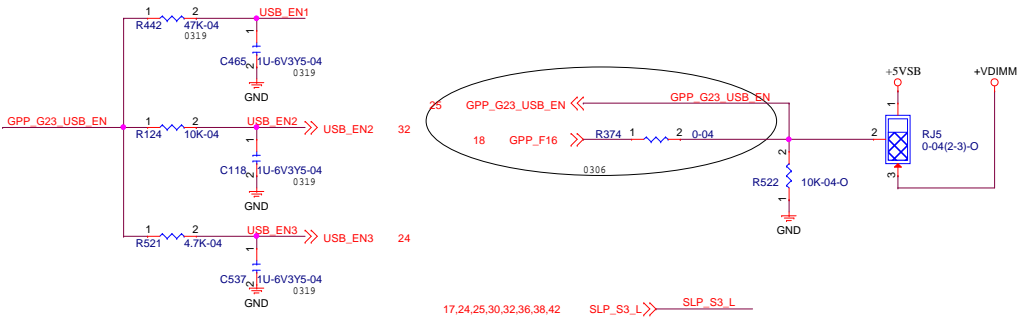


Front IO USB3.0



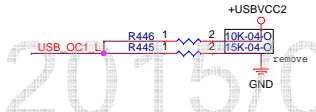
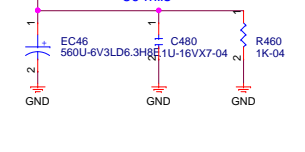
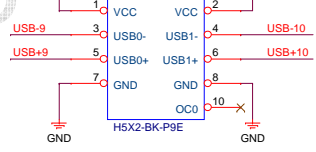
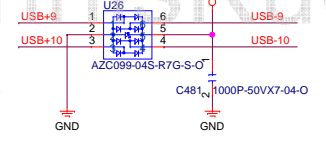
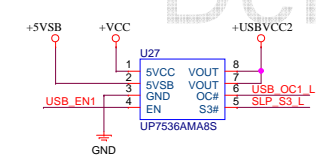
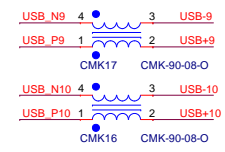
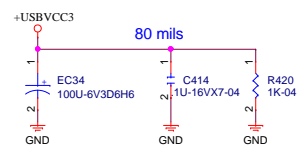
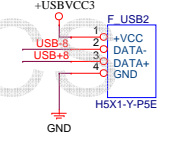
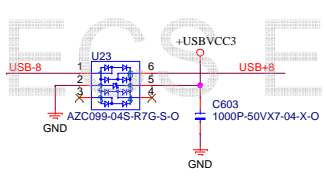
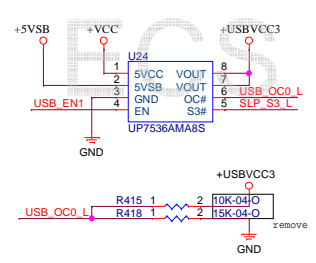
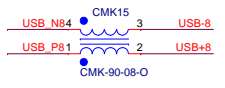
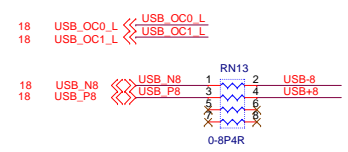


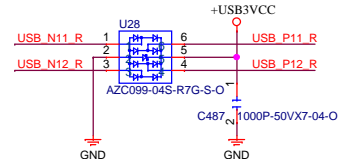
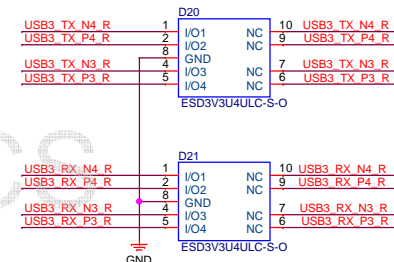
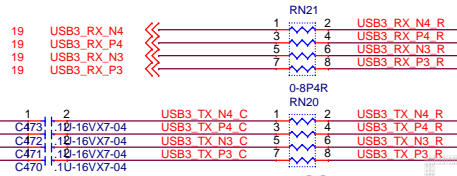
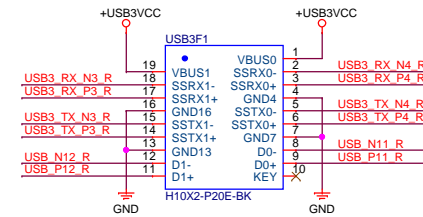
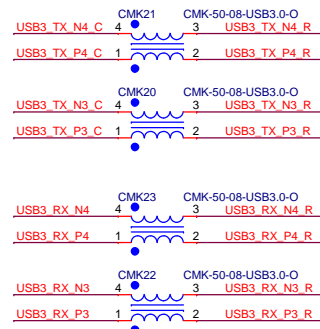
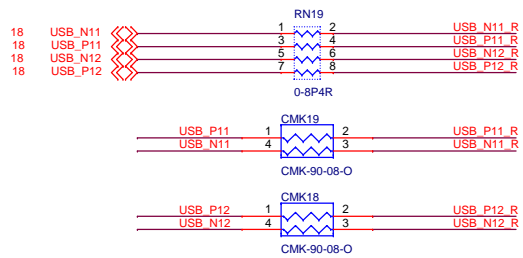




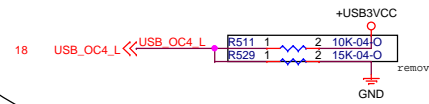
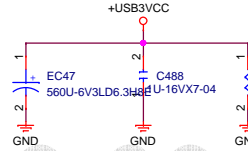
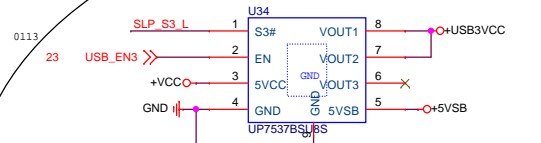
uP7536 Enable use	RJ5	R374	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (2-3)	NA	0 Volt	Acer S4 w/o USB_5VDUAL
5VSB	0ohm (1-2)	NA	5 Volt	
* GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

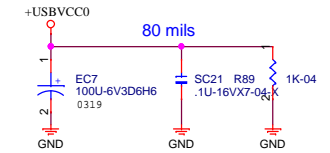
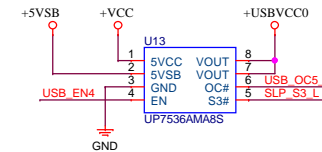
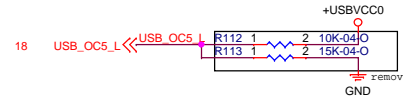
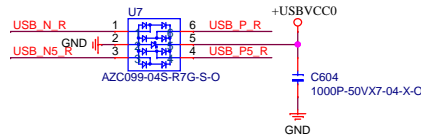
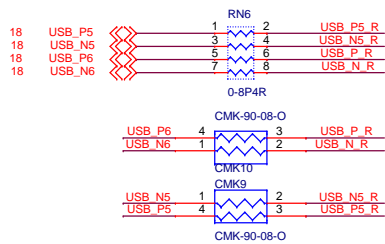
STATUS	S0	S3	S4,S5
GPP_F16	HI	HI	LOW HI
USB_PWR	ON	ON	OFF ON



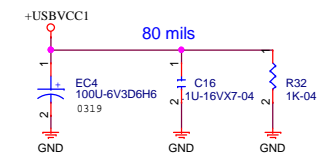
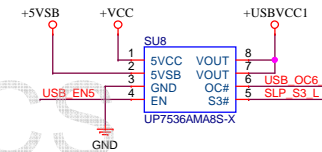
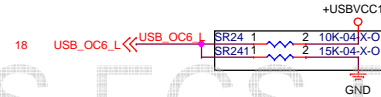
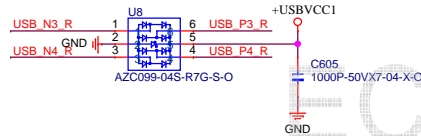
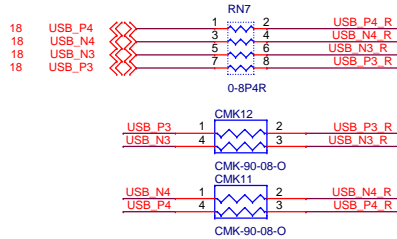


17,23,25,30,32,36,38,42 SLP_S3_L





USB2.0 connector

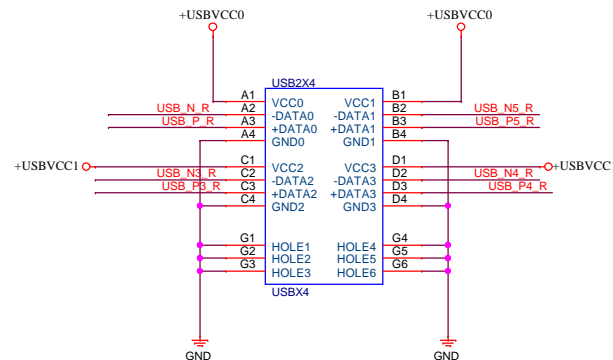
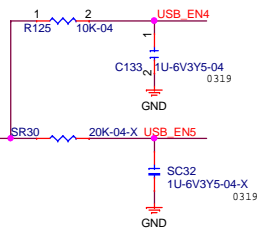


Denniskuo

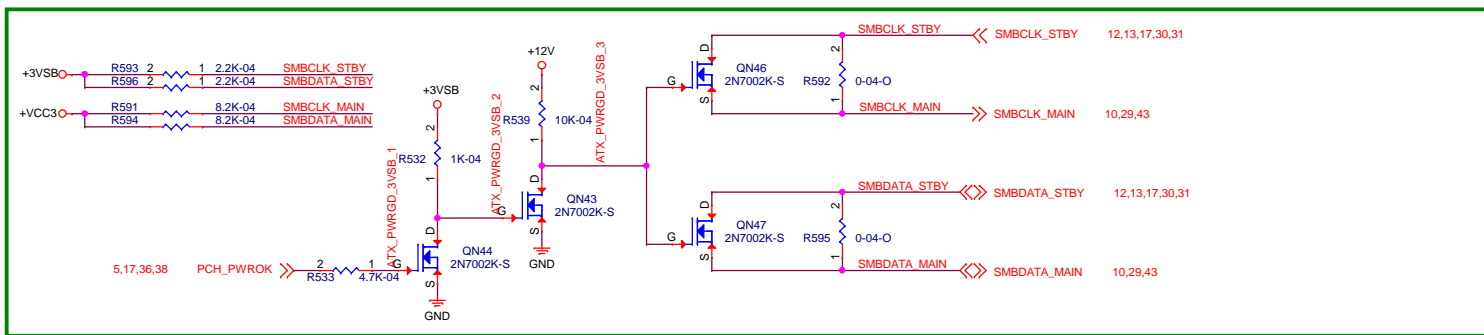
1105

2015/08/26 09:55

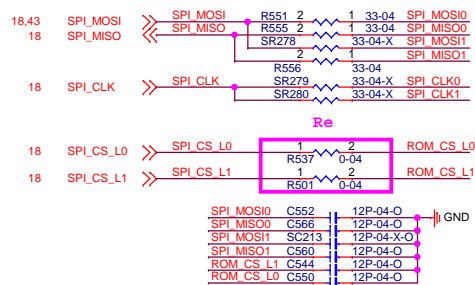
17,23,24,30,32,36,38,42 SLP_S3_L



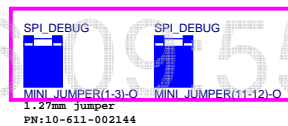
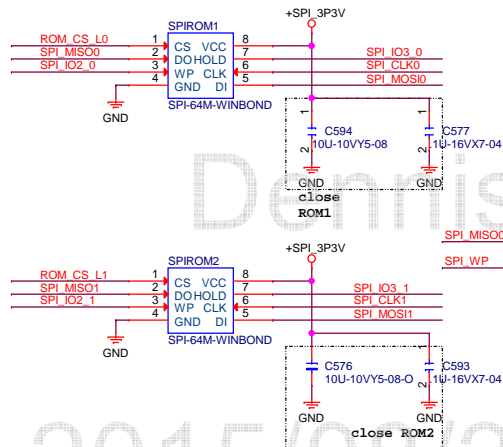
Elitegroup Computer Systems		
Title	USB2.0*4 Connector	
Size	Document Number	Rev
Custom	Q17H4-AD/B15H4-AD	1.1
Date:	Thursday, August 06, 2015	Sheet 25 of 47



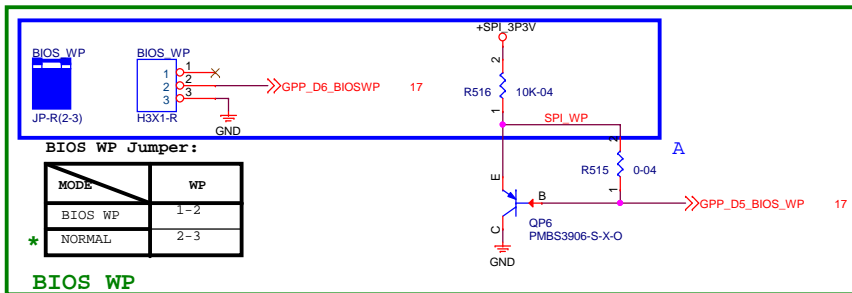
SMBus Logic Circuit



SPI ROM



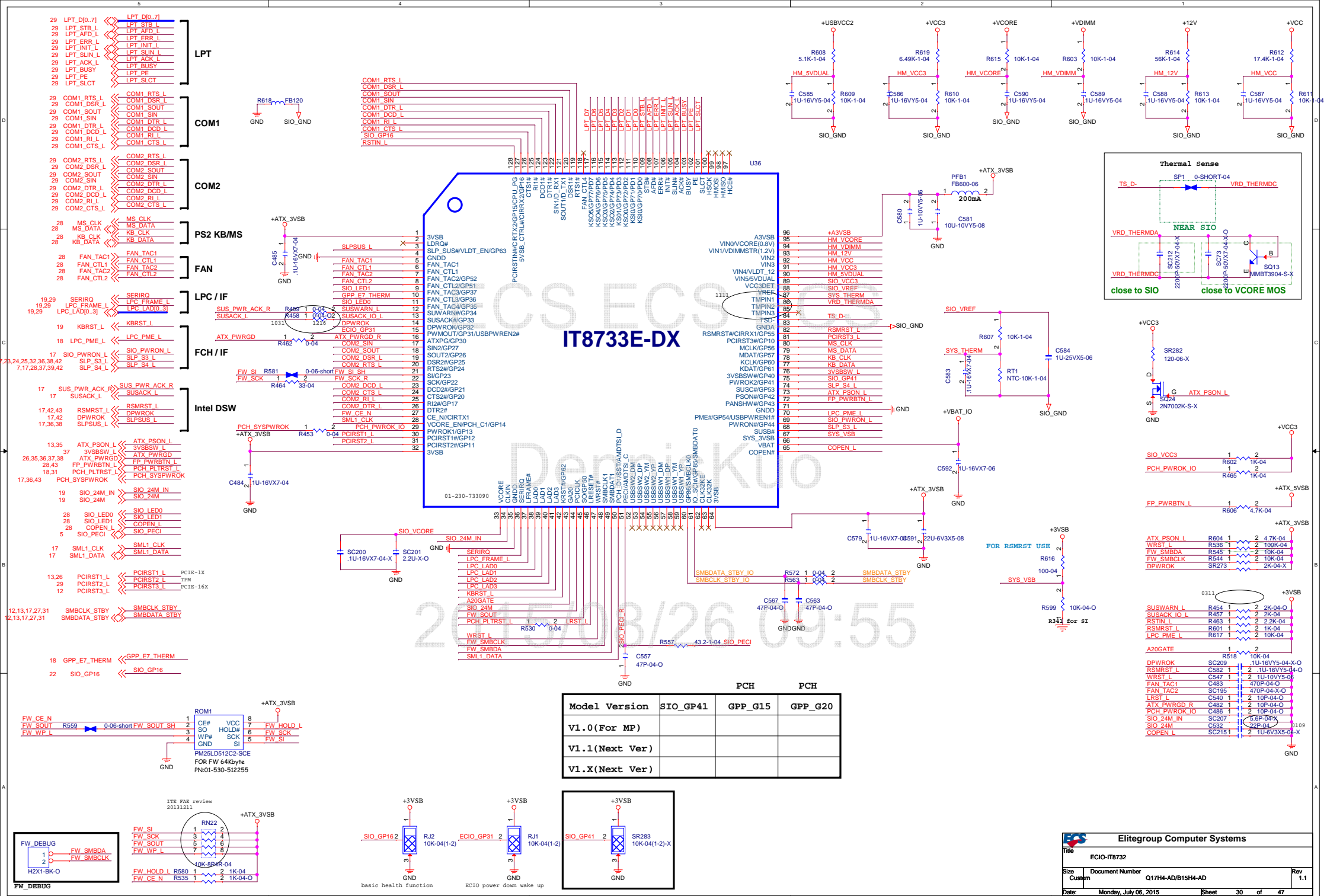
	Ra	Rb	Rc	Rd	Re
A3~A5	O	O	O	O	X
MP	X	X	X	X	O

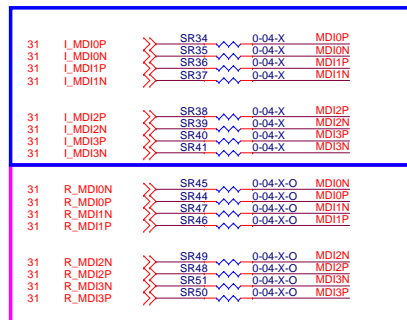
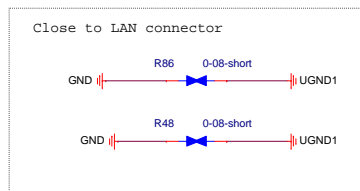
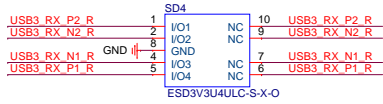
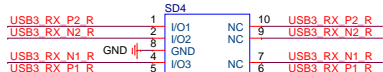
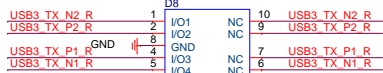
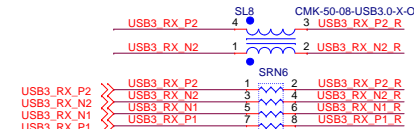
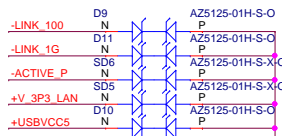
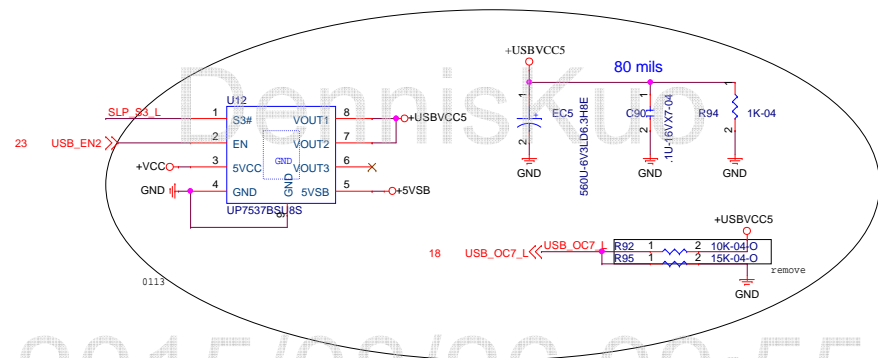
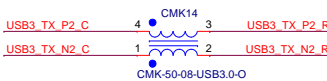
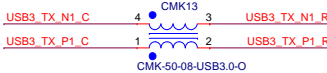
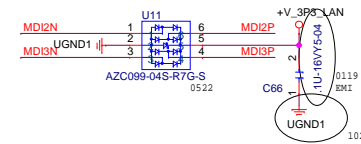
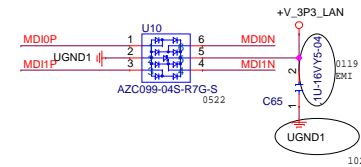
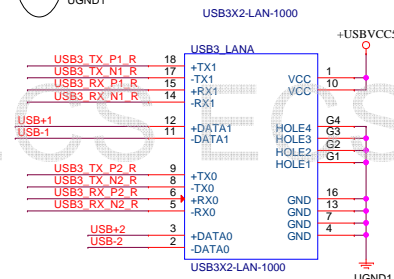
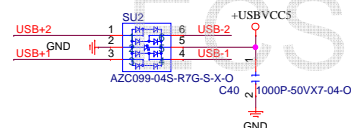
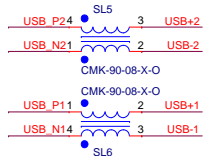
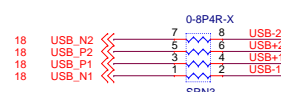




LPT Header circuit





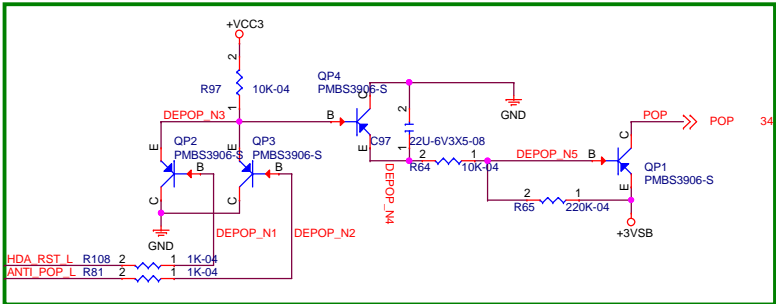
[illegible]

Write down all BIOS Default Settings related to LAN/LKD:

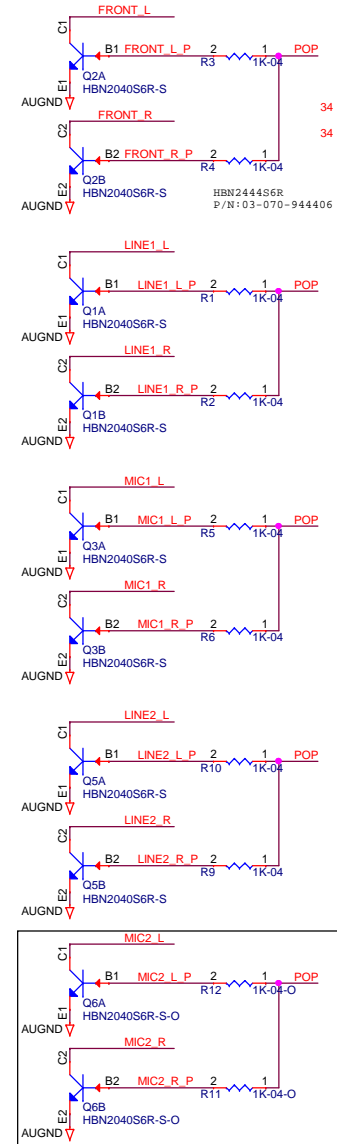
1. EUP, 2. WOL, 3. DASH, 4. LAN Power Control, 5.

			S0	S3	S4	S5	G3 to S5
Front Side	LAN LED (Active LED, Single Color)	Access Not Access	Blank OFF	OFF	OFF	OFF	Dark Case
Rear Side	Active LED (Single Color)	Access	Blank	Blank	Blank	Blank	
		Not Access	OFF	OFF	OFF	OFF	
	Speed-LED (Dual Color)	Disconnected	OFF	OFF	OFF	OFF	
		1000: ON with Amber Color	ON				
		100: ON with Green Color	ON				
	10: Off	OFF					

1. Test under BIOS Default Value only
2. Turn off the front Active LED during S3, 4, 5
3. Once there is packet access or pin, the active LED blanks; otherwise, it turns off.
4. The table also for the functions of EUI³, WOL, DASH or AMT⁴ and so on. Just follow the above criteria based on the real situation for each ACPI state.

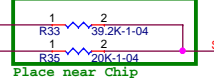


De-pop circuit

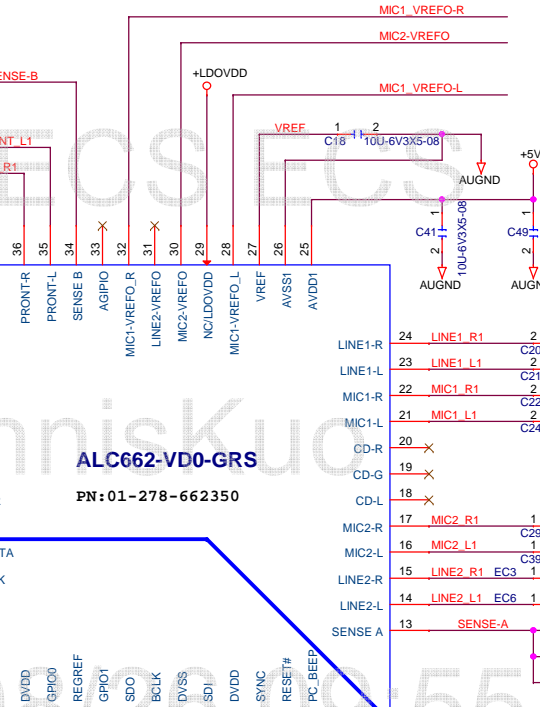
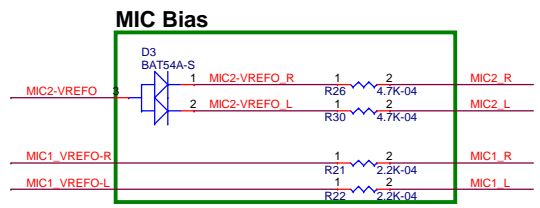


default :reserve for Acer

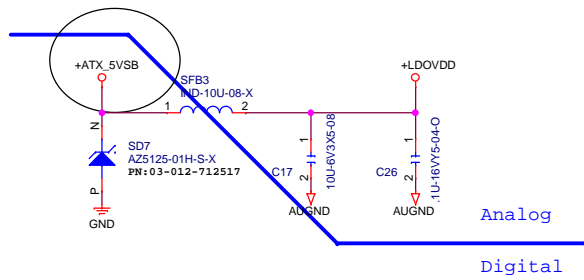
Resistors Networks



Place near Chip



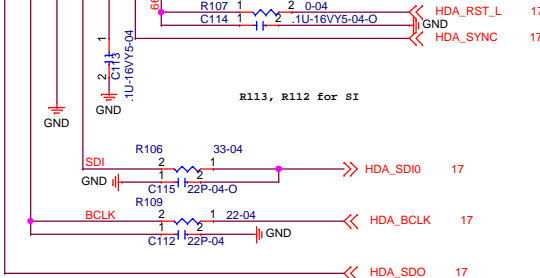
ALC662-VD0-GRS
PN:01-278-662350




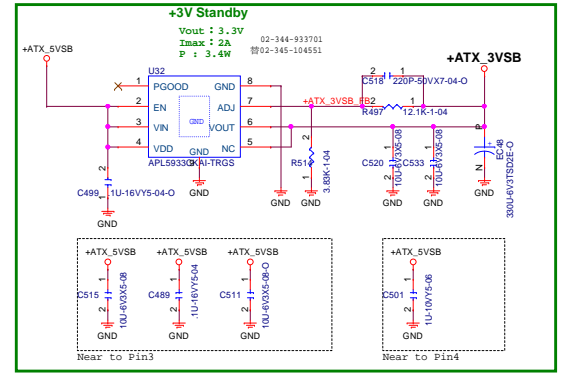
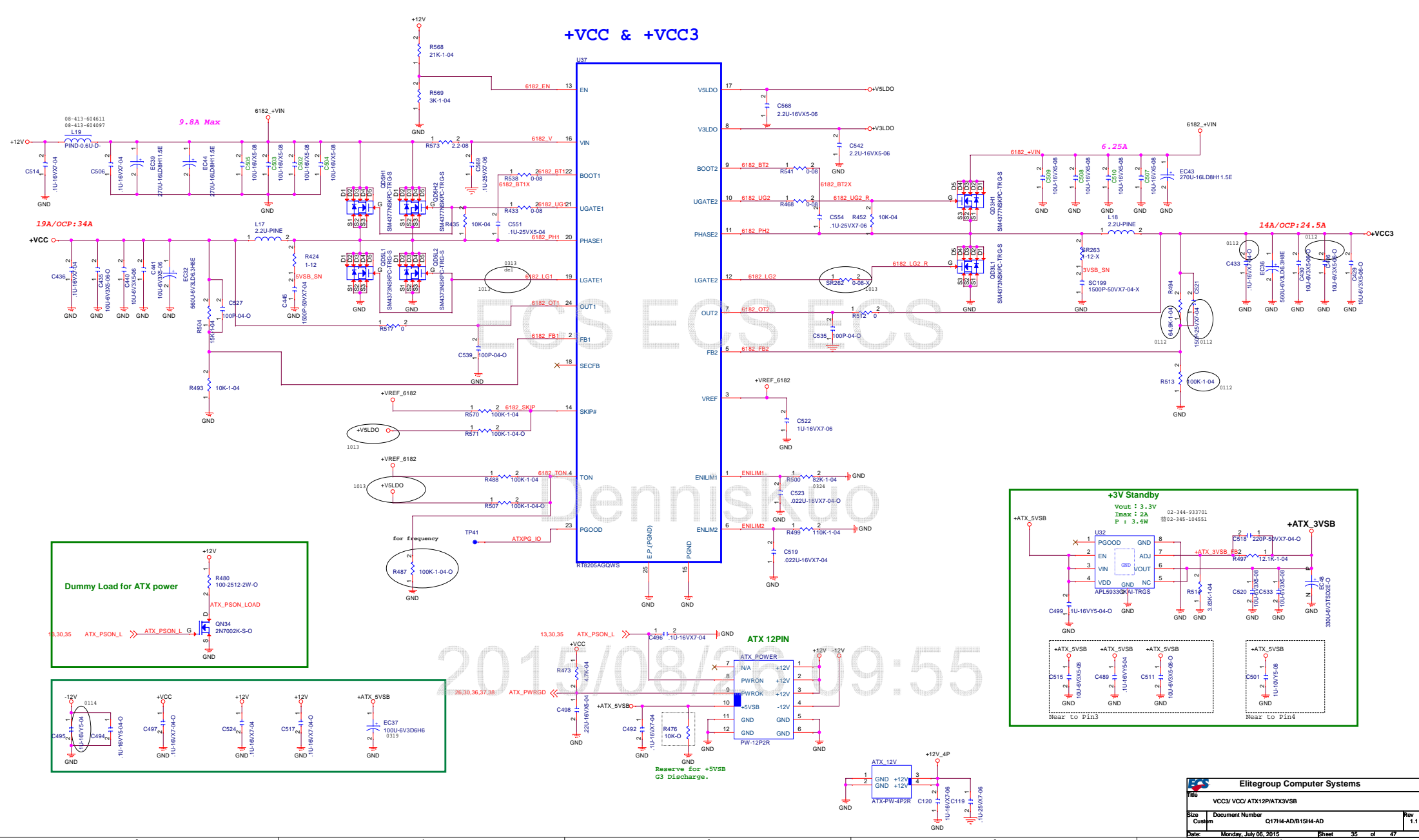
Resistors Networks



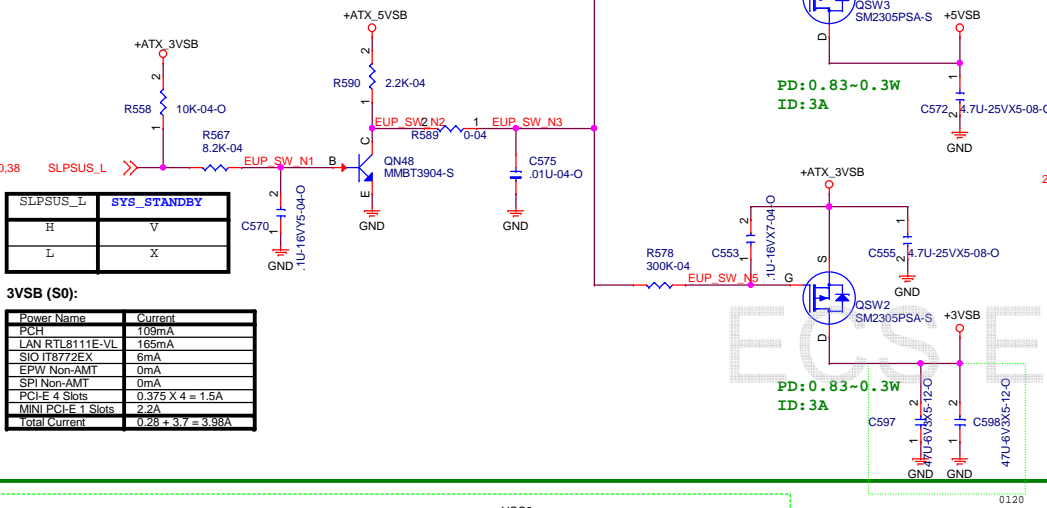
Place near Chip



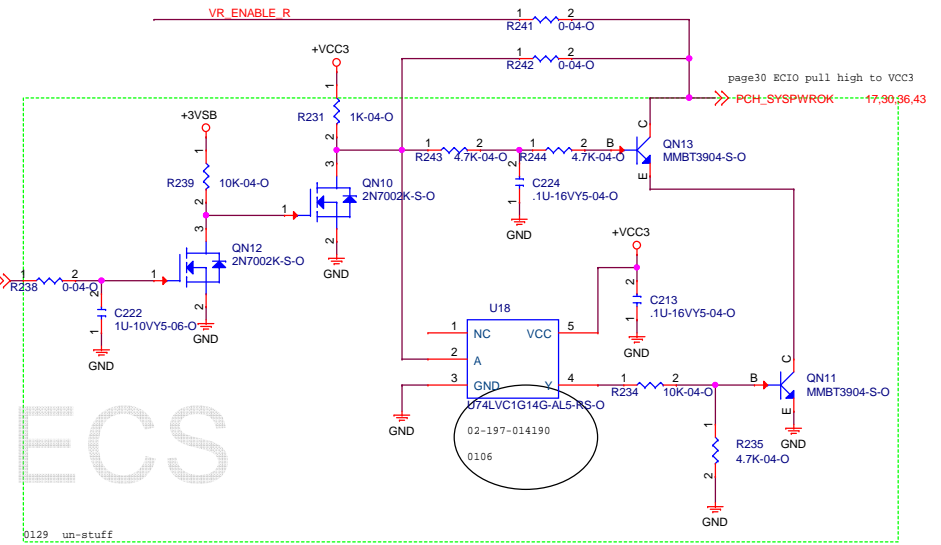
 Elitegroup Computer Systems			
Title			
AUDIO-ALC662_VD			
Size	Document Number		Rev
Custom	Q17H4-AD/B15H4-AD		1.1
Date:	Monday, July 06, 2015	Sheet	33 of 47



EuP Lot6 Power Saving Circuit

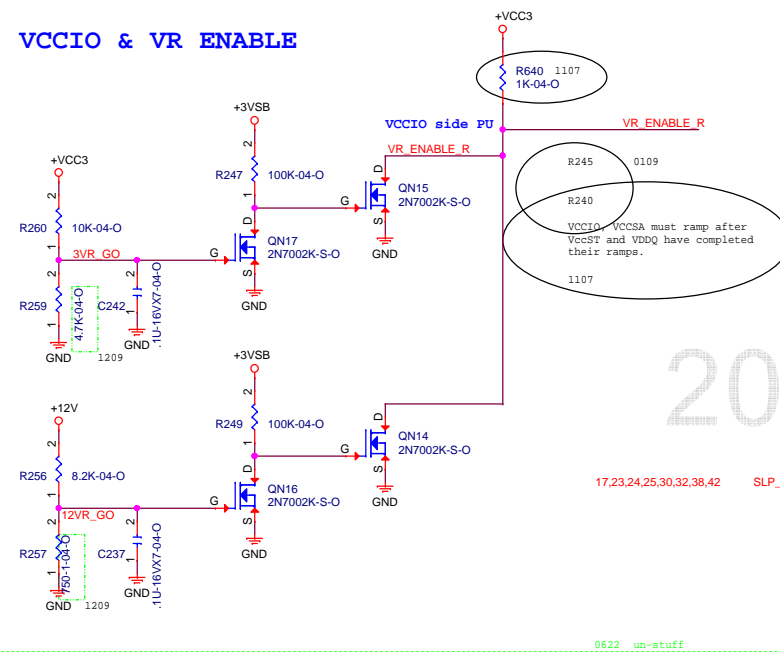


PCH_SYSPWROK POWER DOWN TRIGGER



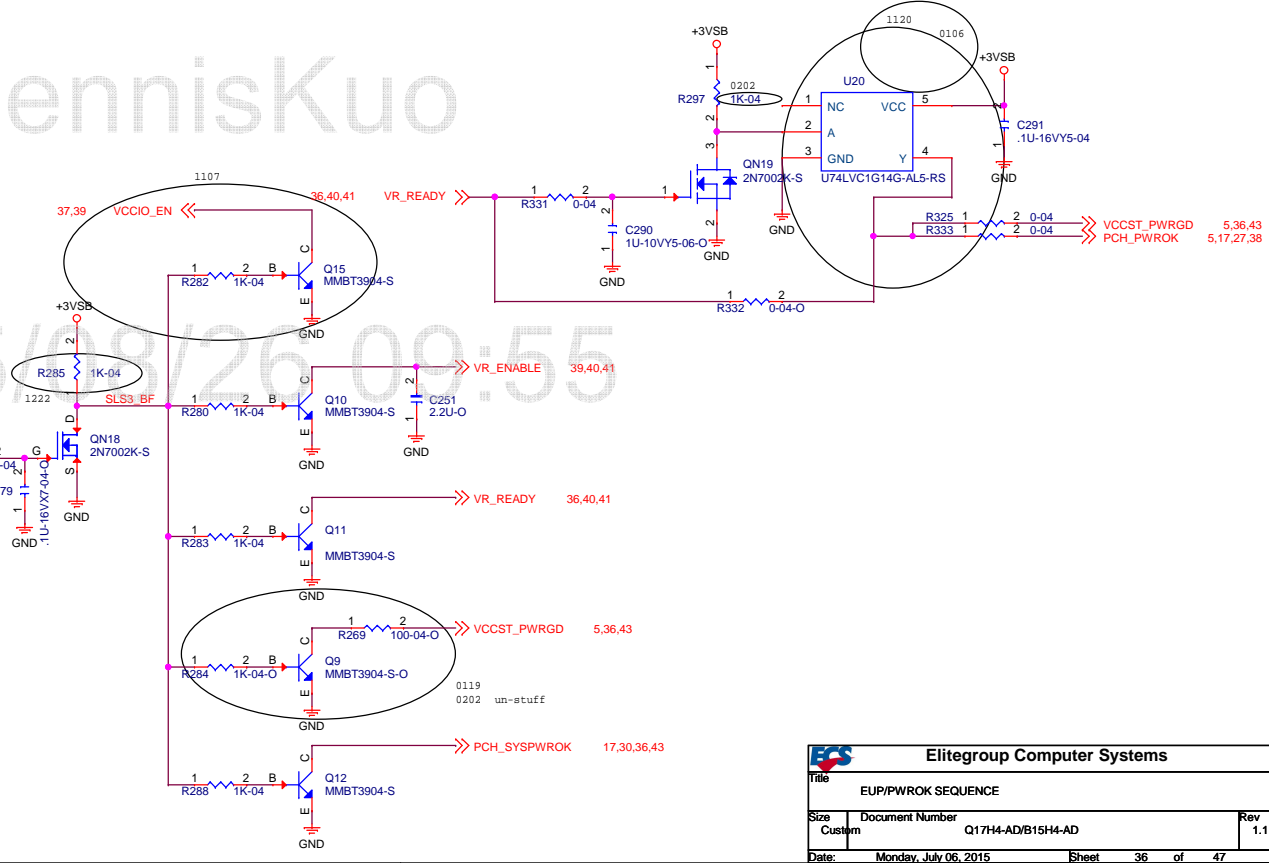
PCH_PWROK & VCCST

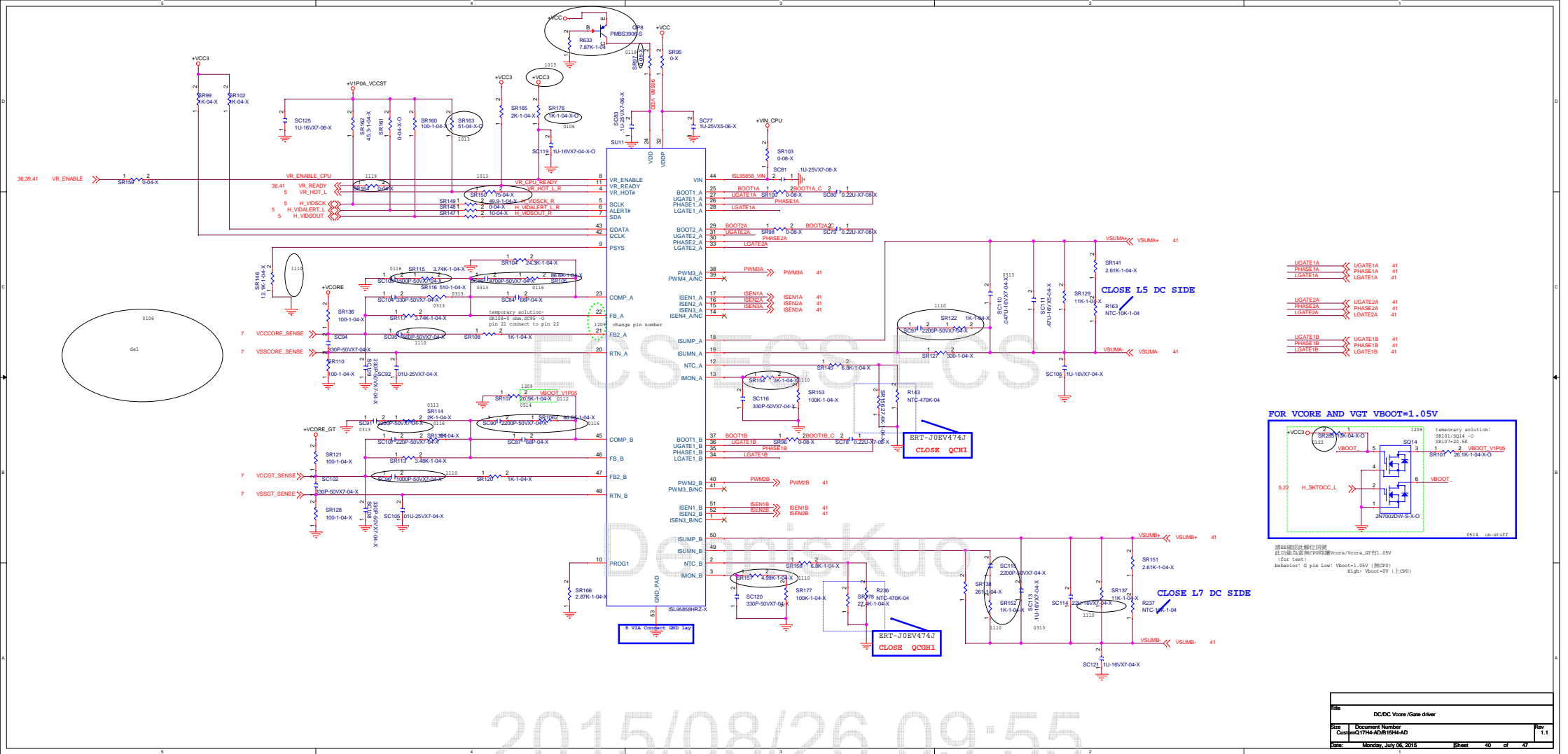
VCCIO & VR ENABLE

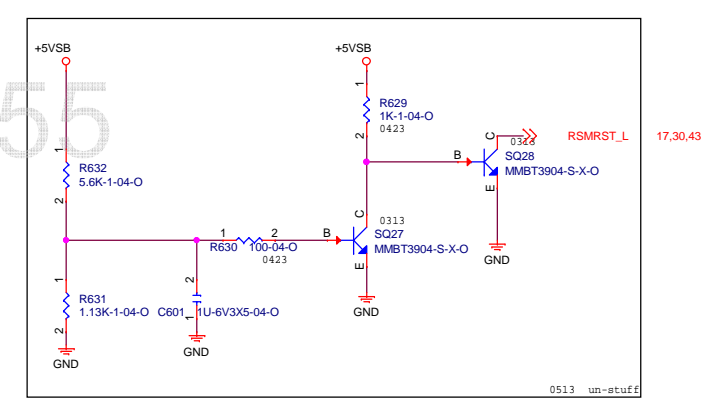
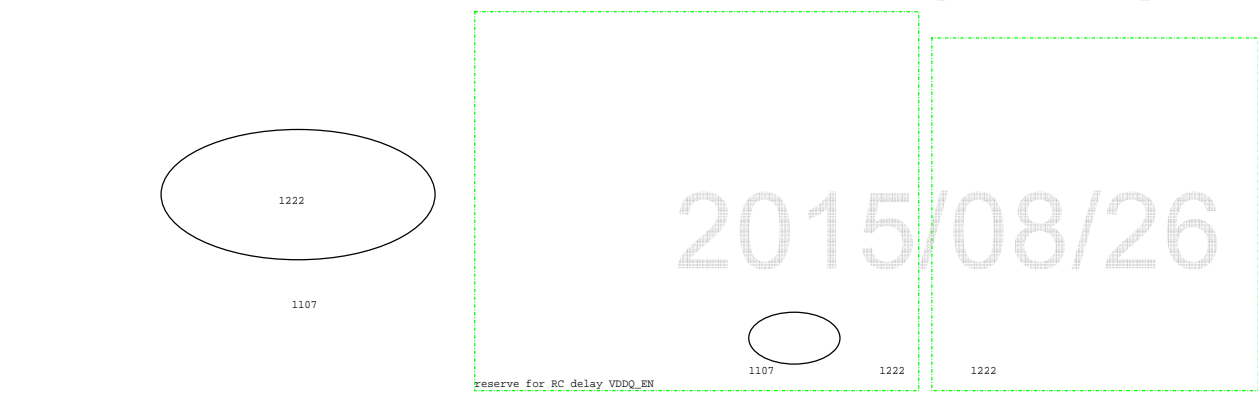
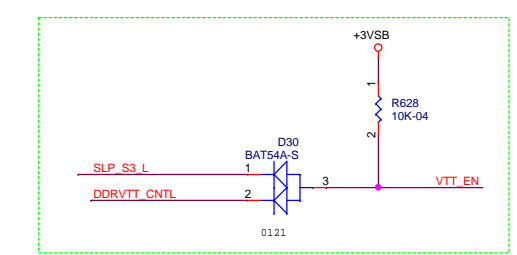
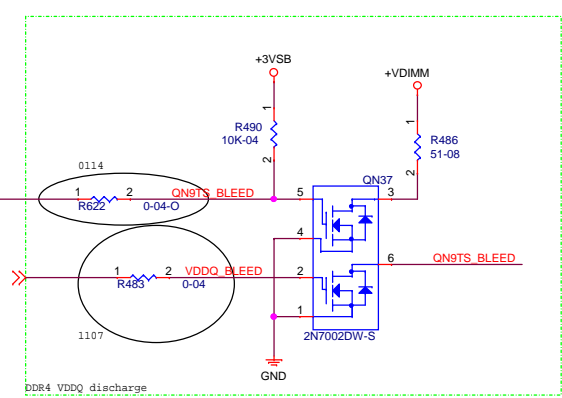
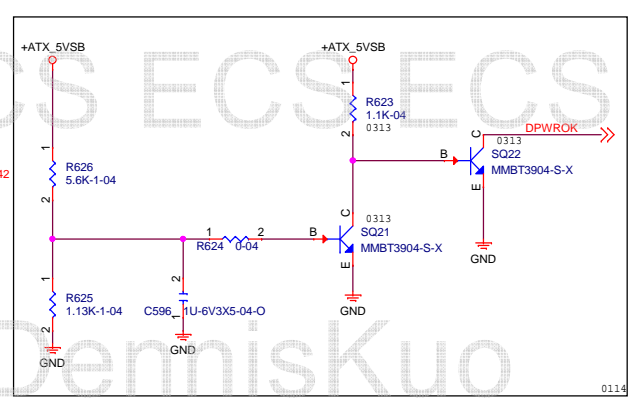
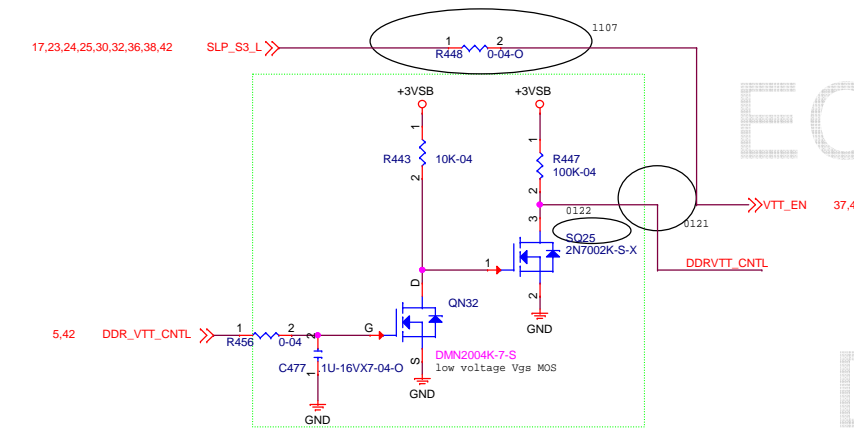
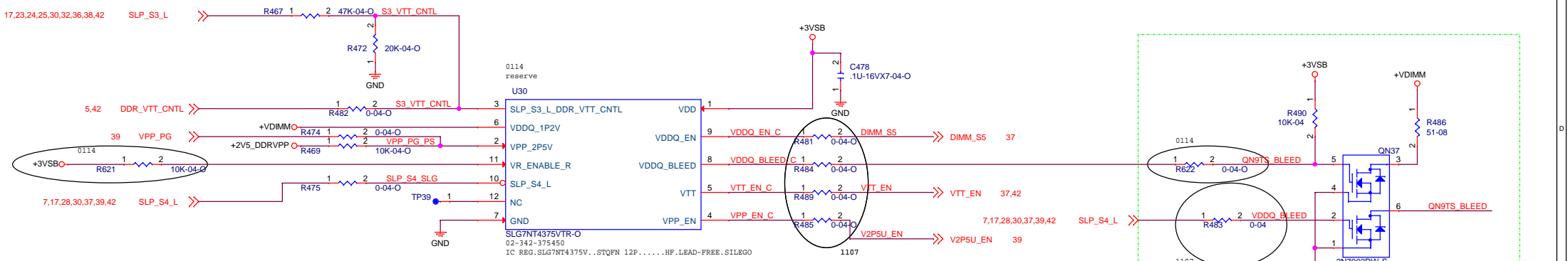


Denniskuo

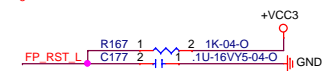
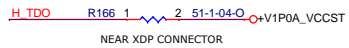
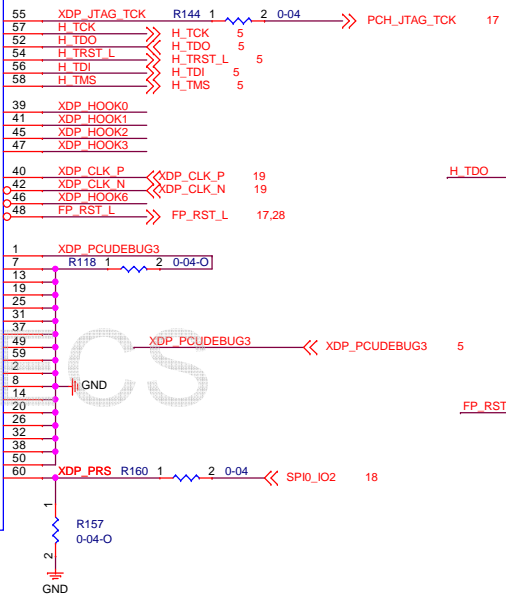
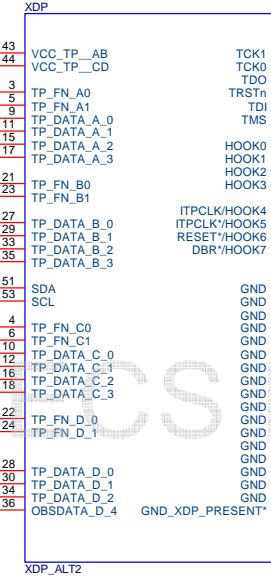
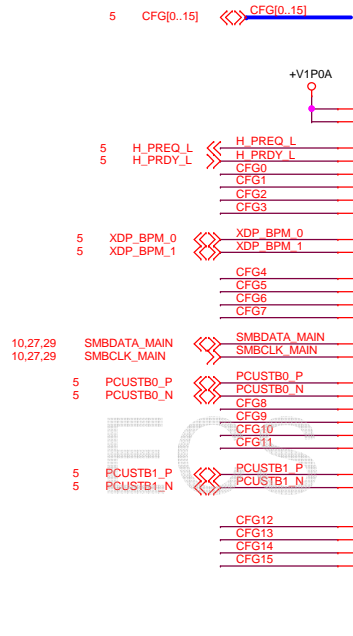
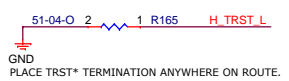
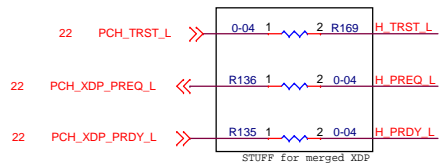
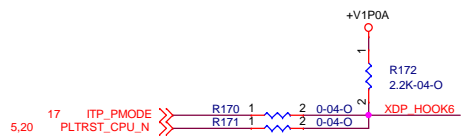
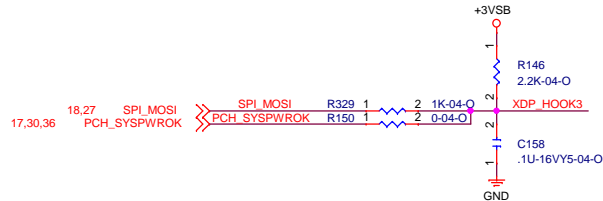
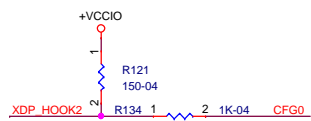
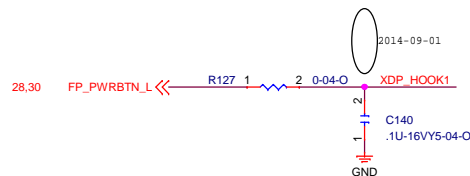
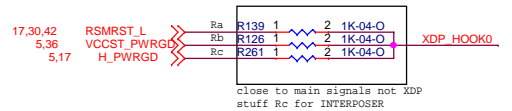
2015/08/26 09:55



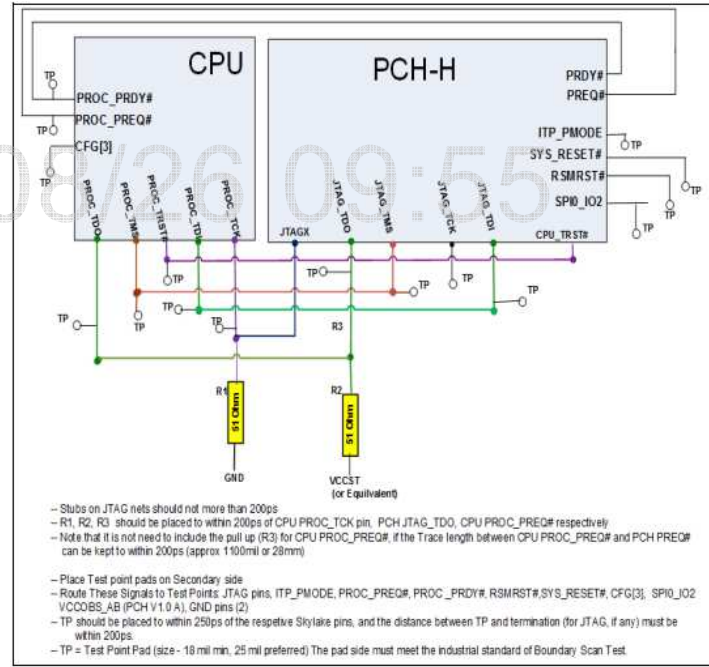




Title		
DC/DC Vcore /Gate driver		
Size	Document Number	Rev
Custom	Q17H4-AD/B15H4-AD	1.1
Date:	Monday, July 06, 2015	Sheet 42 of 47



Stuff XDP
HOOK0 : RSMRST -->R139
HOOK1 : PWRBTN -->R127
HOOK3 : PWROK -->R150
HOOK6 : PLTRST -->R171



ATX SINGLE P/S	
5VSB +/-5%	12V +/-5%

ATX4P
12V +/-5%

Switching ISL95855

Switching APW8727L

Switching RT8207

Switching APW8804

5VDUAL P/N MOS

Switching RT8205A

5VDUAL P/N MOS

Switching APW8727L

3VDUAL

5VDUAL UP7537

5VDUAL UP7536

Intel SkyLake CPU		
VCORE	SVID	70A(65W)
VCC_GT	SVID	37A
VCC_SA	0.95V	10A
VCCIO	0.95V	5.5A
VDIMM	1.2V	2.5A

DDR4 DIMM	
VDIMM	11A(TDC)
VDIMM_VTT	1A
VPP	2.24A

Intel PCH-H (Q170/B150)		
VCCPRIM_1p0	1V	6.15A
VCCCLK1	1V	0.035A
VCCCLK2	1V	0.204A
VCCCLK3	1V	0.058A
VCCCLK4	1V	0.036A
VCCCLK5	1V	0.008A
VCCMPHY_1p0	1V	4.09A
VCCHDAPLL_1p0	1V	0.008A
VCCMPHYPLL_1p0	1V	0.025A
VCCPCIE3PLL_1p0	1V	0.037A
VCCUSB2PLL_1p0	1V	0.013A
VCCPGPPA	3.3V	0.088A
VCCPGPPBCH	3.3V	0.273A
VCCPGPPD	3.3V	0.106A
VCCPGPPEF	3.3V	0.141A
VCCPGPPG	3.3V	0.132A
VCCSPI	3.3V	0.013A
VCCATS	3.3V	0.007A
VCCHDA	3.3V	0.075
VCCPRIM_3p3	3.3V	0.370
VCCDSW_3p3	3.3V	0.502A
VCCRTCPRIM_3p3	3.3V	0.001A
VCCRTC	3.0V	0.001A

2.06A for Deep Sx

LAN Jacksonville I219LM		
VDD3P3	3.3V	164mA

LAN RTL8111EPV		
VDD3P3	3.3V	270mA

FAN		
CPU_FAN	+12V	1A
SYS_FAN	+12V	1A

Battery 3V

SIO IT8733		
3VSB	3.3V	14mA
VCC3	3.3V	TBD
Battery 3.3V	3.3V	2uA

AUDIO ALC662-VD		
DVDD 3.3V	3.3V	11mA
AVDD	5V	42mA
Internal LDO		

SSD/wriess LAN M.2 Slot per	
3.3V	2.5A(S0)

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

SATA power per	
12V	1A
5V	1A

each USB3.0	
5VDual	0.9A

each USB2.0	
5VDual	0.5A

PS/2
5VDual 275mA

